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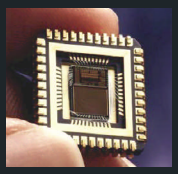
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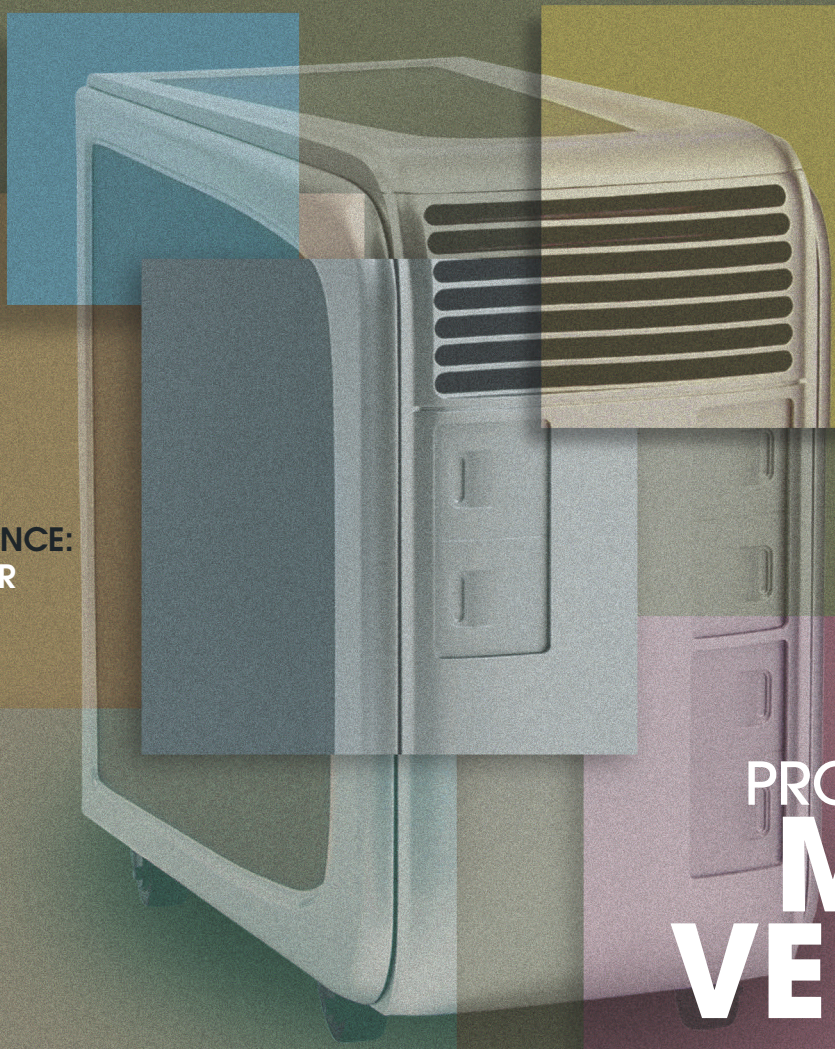


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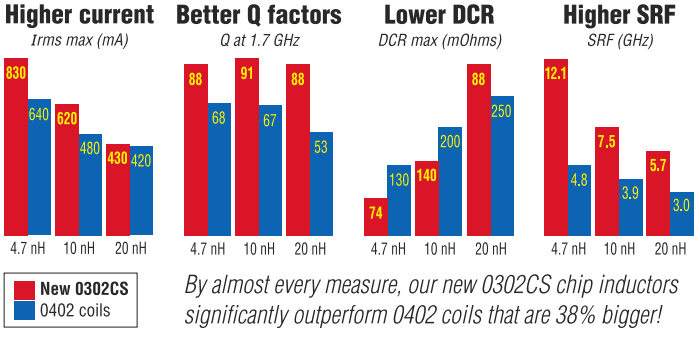
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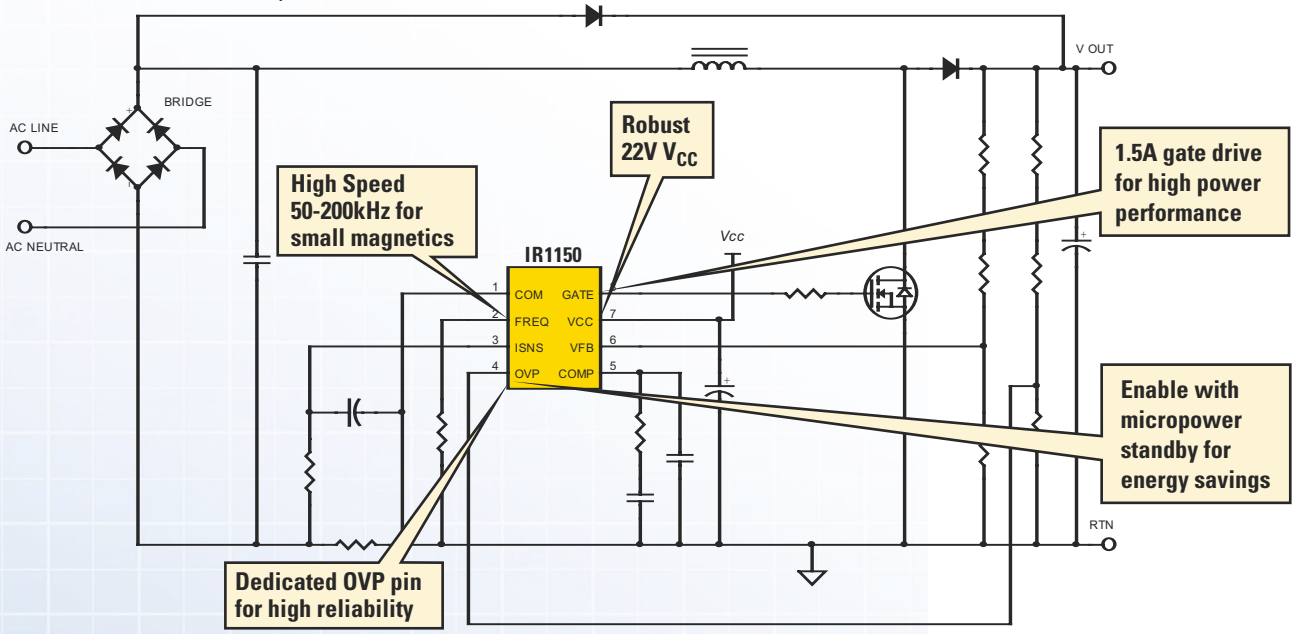
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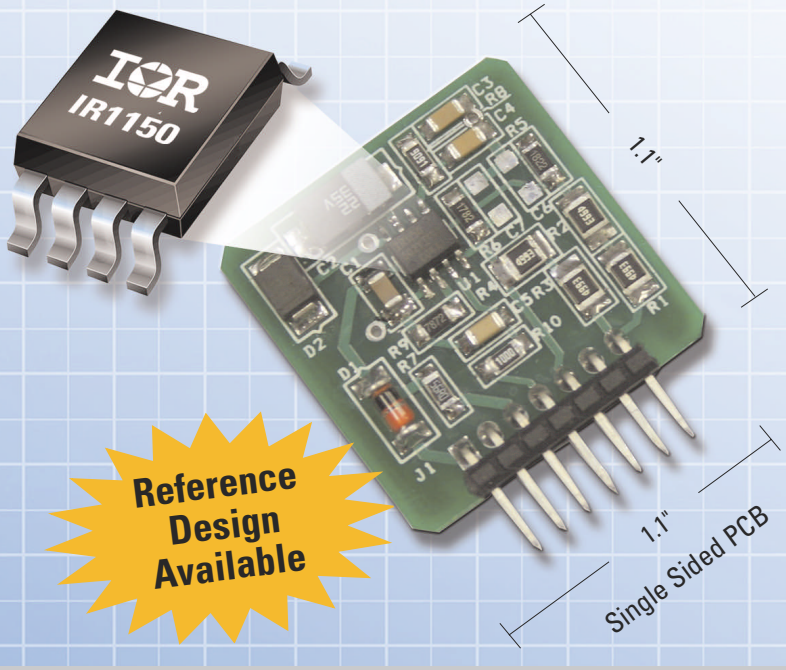
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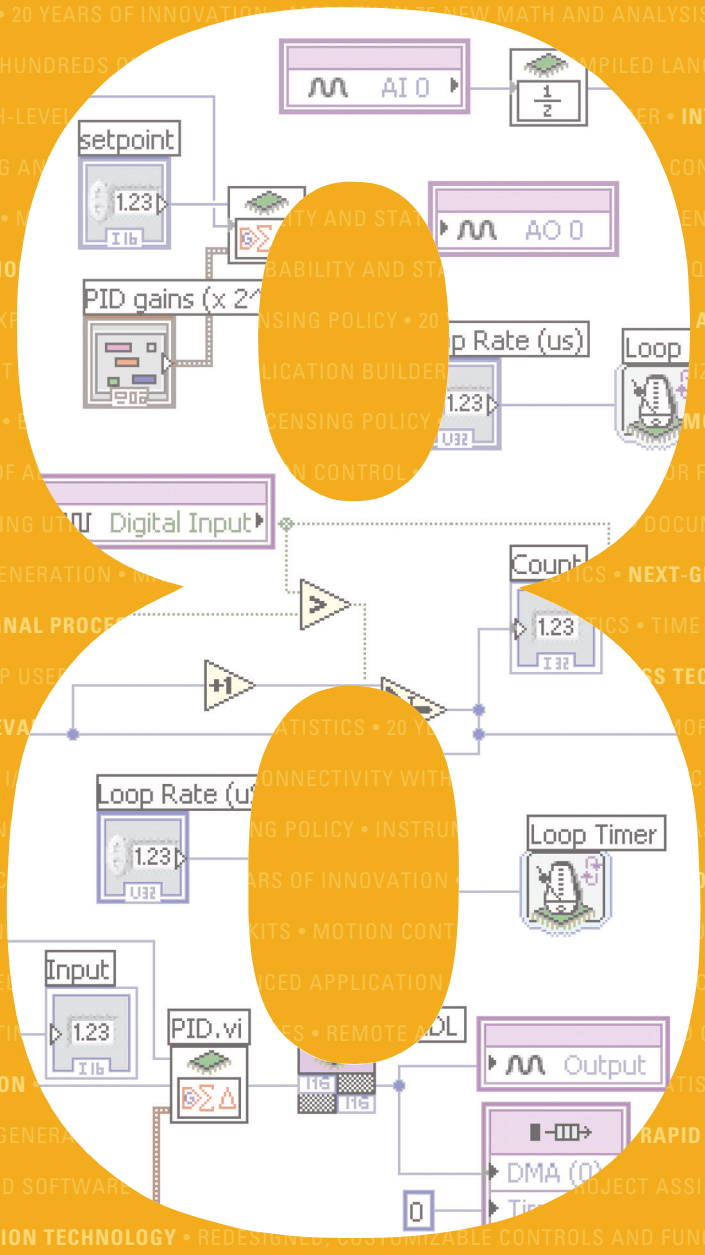
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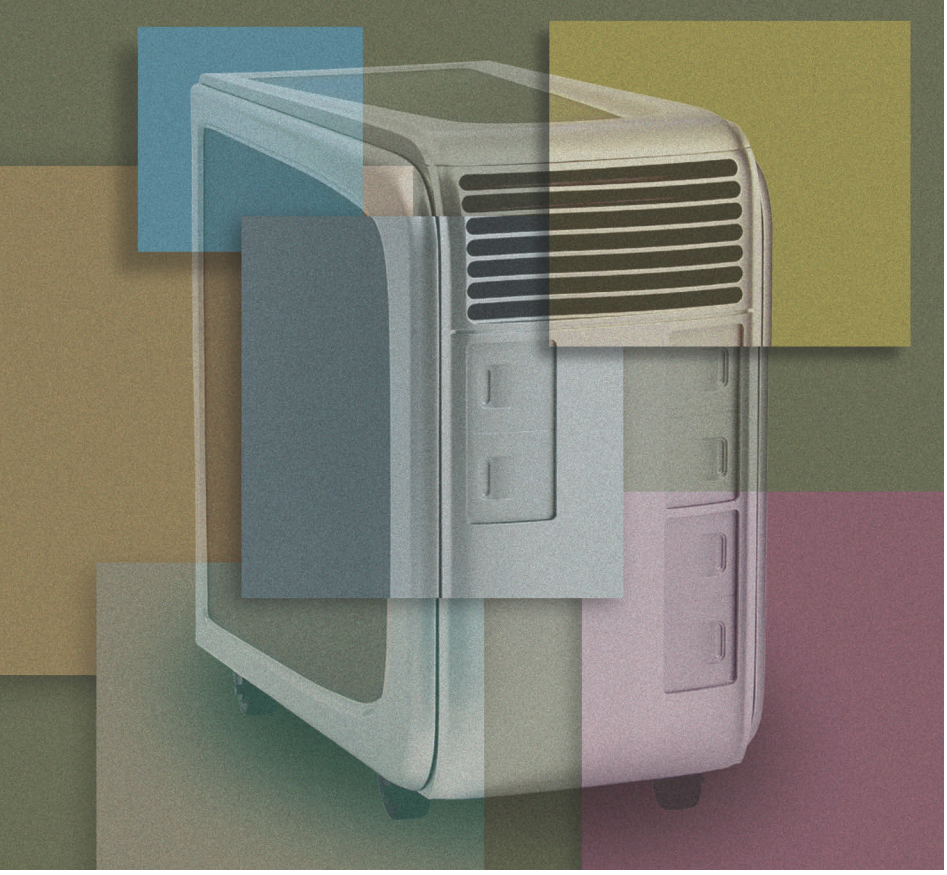
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ASIC prototyping: make versus buy

30 As digital-IC designs have become more complex, so too, has the task of verifying their functions. Over the years, EDA vendors have done little to reduce the gap between the number of gates you can design and the number you can verify in a reasonable amount of time. *by Michael Santarini, Senior Editor*

Mobile robots get serious

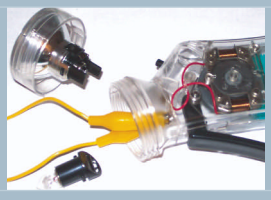
43 After years of serving hobbyists and movie-makers, a series of world events may elevate mobile robots to technology's "next big thing." *by Warren Webb, Technical Editor*



A matter of balance: line-receiver CMR in real-world environments

53 Few applications allow you to control the source impedance of your incoming signals, yet your line receiver's CMR can hang in the balance. *by Joshua Israelsohn, Contributing Technical Editor*

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65 Stereo-amplifier IC's outputs drive multiple loads

66 Muscle power drives battery-free electronics

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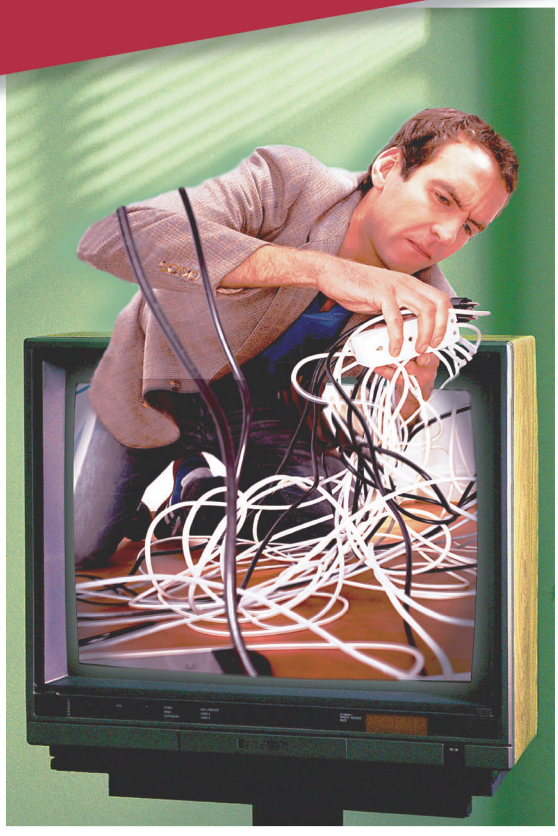
80 **Embedded Systems:** Linux-distribution suite, CompactPCI subsytem, and more

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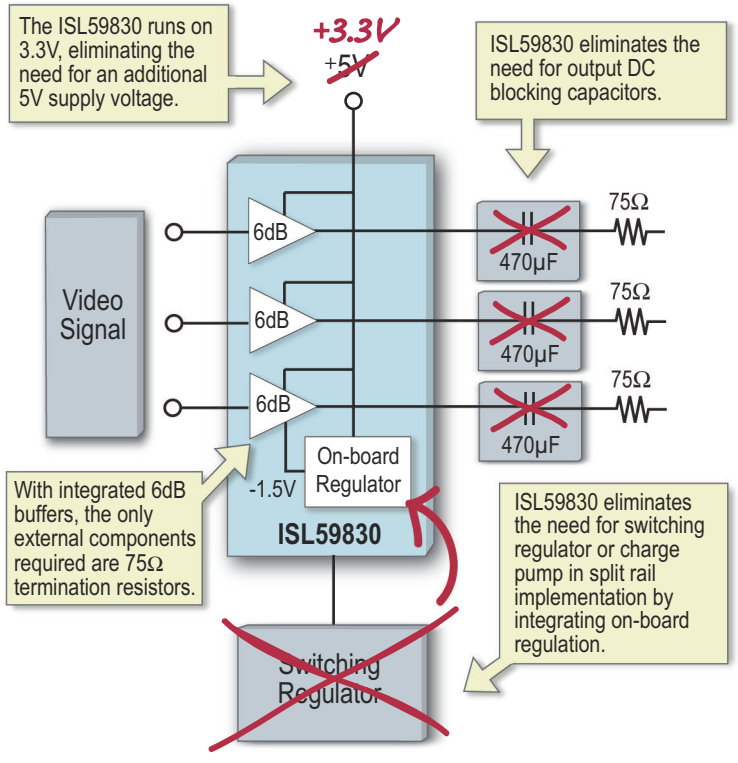
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By Mark Gehring, Cypress Semiconductor

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Mentor Graphics says it hasn't discontinued but has rather "de-emphasized" its FormalPro equivalence checker.
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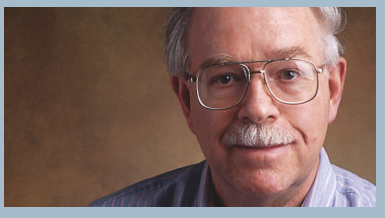
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BY JOHN DODGE

No nation left behind—by electronics

As markets saturate in developed nations, the focus turns to emerging economies to pick up the slack. But two recent initiatives to help the poor nations—creating a less-than-$30 mobile phone and a $100 laptop—fall into the category of good works.

As the names of these initiatives imply, cost is a foremost concern. A $100 mobile phone and $150 average bill won't go over well in East Timor, where annual per capita income is $400. And in underdeveloped countries that lack power sources for recharging, a single charge must last a long time.

The GSMA (Global System for Mobile communications Association) announced in July a highly publicized contest to develop a less-than-$30 mobile phone. Motorola won Phase One of the contest with its model C113a handset due out in the first quarter of 2006.

The C113a promises 340 to 700 minutes of talk time and 175 to 450 hours of standby time on a single full charge (**Link 1**). Its squarish looks won't win any beauty contests next to slick Moto Razr, but the unit offers all the basic mobile-phone features.

The GSMA estimates that a low-cost handset could add 1 billion more users to the 1.5 billion GSM users worldwide today. ABI Research expresses the opportunity another way. Four-fifths of the world's population lives within reach of a cellular network, but only 25% tap into it; hence, the drive for the low-cost phone. Only Nokia and Motorola have come out strong in this competition, and handset makers ignoring this low end of the market do so at their own peril, warns Alan Varghese, principal semiconductor analyst at ABI.

"Some manufacturers prefer to do smart phones and enhanced feature phones because they are more profitable. But that argument does not work in cellular because it's about how many millions of units are you doing. If you don't play, that means your volumes are lower, and you don't get the pricing advantages from your suppliers."

The less-than-$30 phone is the easy part of providing mobile-phone service to developing nations, according to Johan Wall, chief executive officer of Enea, a Swedish developer of embedded real-time operating systems for phone makers such as Nokia and Ericsson. "The challenge is building the mobile infrastructure that can get the monthly bill down to $5 to $7."

The other effort to serve cost-constrained sectors, such as education and developing countries, is the $100, Linux-based laptop under development at the Massachusetts Institute of Technology's Media Lab (**links 2** and **3**). The only thing it can't do that a $1000 laptop can is store massive amounts of data, according to MIT. Specs include USB ports, WiFi, and a 500-MHz to 1-GHz processor. Its answer to scarce electricity sources is a built-in hand-cranked charging unit.

Cost-wise, the tricks are getting the display to less than $35; stripping out the fat, such as software overhead; and producing the laptop in huge quantities. MIT plans to market the $100 laptop to ministries of education under the "One Laptop per Child" program and says shipping will begin as early as next year once the lab receives 5 million to 10 million paid orders. MIT officials claim that they've held discussions to place orders with Brazil, China, Thailand, and Egypt.

Such volumes at first might seem a bonanza for component suppliers, but increased integration and tremendous cost pressures cancel out correspondingly more profit. After all, we already have single-chip cell phones. At Nokia, average parts per phone topped out at 400, but have since settled back to about 320, according to Nokia Procurement Chief Jean François Baril (**Link 4**).

A $100 laptop can't be good news to companies such as Dell and Hewlett-Packard, even though MIT hasn't disclosed any plans to market the devices to the general public. Still, a less-than-$30 mobile phone and $100 laptop are good news for places unaccustomed to it. EDN

WEB LINKS

1. www.motorola.com/motoinfo/product/images/0,,124,00.html.
2. http://laptop.media.mit.edu/.
3. www.spinellis.gr/blog/20051014/.
4. www.reed-electronics com/moversandshakers.

EDITOR'S NOTE:

This is the final EDN *column for John Dodge, who is now editor in chief of sister publication* Electronic Business. *The* EDN *staff wishes John well and thanks him for all he taught us about voices in* EDN. *You can expect to see closer cooperation—especially on the Web—among* EDN, Electronic Business, Electronic News, *and other Reed Business Information titles.*

I have stepped back into the editor-in-chief spot at EDN, *and I look forward to engaging with you. Please email me with your opinions about what we're doing wrong and right.*

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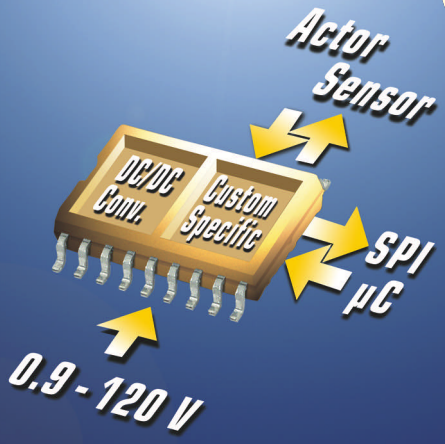
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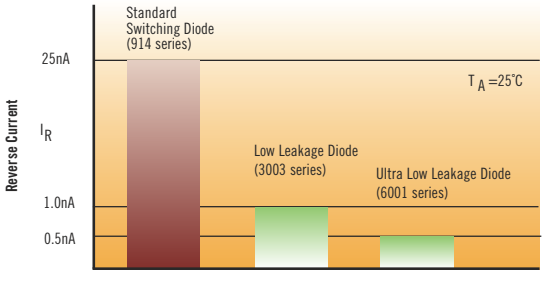
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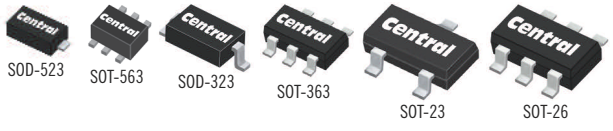


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Motion controller boosts servo-loop rate

Targeting high-performance applications in the medical, scientific, and automation industries, Performance Motion Devices recently announced the Magellan-PCI motion controller featuring a servo-loop rate of 50 μsec per axis. Available in one-, two-, three-, and four-axis versions, the Magellan-PCI supports dc-brush, brushless-dc, microstepping, and pulse and direction motors. Magellan-PCI provides a 5 million-count/sec quadrature-encoder input rate and pulse and direction output as high as 5 million pulses/sec. Other features include trajectory generation, servo-loop closure, quadrature-signal input, motor-output signal generation, servo trace, on-the-fly changes, and commutation. Board-communication options include the CANbus, a serial port, and the PCI bus.

With the onboard Magellan motion processor, designers can create high-performance motion systems using standard C or C++ programming. The card accepts input parameters, such as position, velocity, acceleration, deceleration, and jerk, and automatically generates the programmed trajectory. Designers can perform on-the-fly changes and use external signal-I/O breakpoints to create application-specific profile changes. Magellan-PCI is available now with prices starting at $638 (OEM quantities).

—by Warren Webb

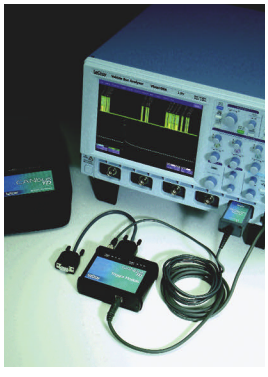
▷**Performance Motion Devices Inc**, www.magellan-pci.com.



The Magellan-PCI delivers servo-loop rates of 50 μsec per axis to dc-brush, brushless-dc, microstepping, and pulse and direction motors.

Vehicle-bus analyzer decodes CAN in symbolic format

LeCroy's new VBA (vehicle-bus-analyzer) oscilloscopes decode CAN (controller-area-network) serial data into symbolic application-layer text. The instruments allow designers of CAN electronic-control units and vehicle networks to view the full range of CAN-protocol-stack information, plus symbolic, hexadecimal, and electrical signals. They also allow designers to use standard and specialized oscilloscope tools to validate and debug designs. The units display in-circuit electrical signals, such as sensor inputs, voltage levels, and transients, that affect the CAN bus; they decode as many as four CAN buses at once.



The 500-MHz and 1-GHz vehicle-bus analyzers decode CAN-bus serial data into symbolic text, greatly reducing the time required for debugging CAN-bus applications.

The four-channel, 500-MHz- and 1-GHz-bandwidth, 5G-sample/sec analyzer scopes offer a standard memory depth of 2M points/channel expandable to 24M points/channel. Prices start at $18,990.

According to Michael Lauterbach, PhD, LeCroy's director of product management, the VBAs extend the CAN-triggering capability that the company previously released in its CANbus TD (trigger-decode) scope option. "Using a CAN-standard DBC [database-container] file that contains information pertinent to the CAN messages and signals, an operator can symbolically select a message or a signal and apply a data condition for triggering," says Lauterbach. "Thus, instead of having to understand how to trigger on an 0x410 message that contains 3f in its second data byte, the operator can quickly consult a predefined list, pick the steering-wheel speed-of-travel signal that is part of the output message, and define the desired data condition. This approach makes trigger setup quick and intuitive, requires little or no cross-referencing to other files or programs, and results in greater operator confidence."**—by Dan Strassberg**

▷**LeCroy Corp**, www.lecroy.com/tm/solutions/automotive/.

Network time server keeps dispersed systems in sync

Don't kid yourself: A basic crystal oscillator on a pc board has significant drift and other variabilities. So, even if you have a precise timing source at each system node, you also need a way to properly synchronize them to the same time (see "Does anybody really know what time it is?" *EDN*, Oct 27, 2005, pg 14, www.edn.com/article/CA6275409). Yet, systems increasingly need more precise and accurate time stamps for logging, debugging, chain-of-events analysis, and electronic-transaction control. A pair of time-server units from Symmetricom provides not only the physical timebase, but also the system-level software and tools to provide, synchronize, and manage the process. The units are compatible with higher speed NGNs (next-generation networks), which developers are designing and deploying for the Internet.

The SyncServer S200 and similar S250 use the atomic clocks within GPS (global-positioning-system) satellites as their primary timebase source and provide for an external antenna. You can add an internal backup cesium clock if you lose GPS visibility. The rack-mount chassis units have three independent 10/100BaseT Ethernet ports with IPV6 support; dual USB ports; the ability to support hundreds of thousands of nodes or network clients with NTP (network-time-protocol) time stamps; a user-friendly, secure, Web-based interface; and a front-panel, multiline, high-resolution, large-character display and full numeric keypad, sure to be a hit with hands-on users. A setup-and-operating wizard simplifies installation and configuration.

The time stamp provides better-than-10-µsec accuracy at NTP rates of 5000 packets/sec; the basic clock is accurate to 50 nsec for UTC (universal-time-code) worldwide synchronization. The S200 targets use in IT applications, and the S250, which also includes synchronization with IRIG (Inter-Range Instrumentation Group) B, one-pulse/sec, and 10-MHz outputs, finds use in NGN applications. Prices range from $3595 to less than $10,000, depending on options and configuration.

—by Bill Schweber

▷**Symmetricom Inc**, www.symmetricom.com.



Keep your dispersed network ready, set, and going in sync using the next-generation-ready S200 and S250 SyncServer time servers, which use GPS timing, an internal crystal, and an optional atomic source.

FEEDBACK LOOP

"Spreading the emission around is not a solution to low-EMI design. It is cheating by exploiting the limitations of test equipment. Don't follow this Trojan horse—*burn it down*!"

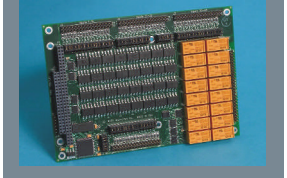
Robert C Mooney in *EDN*'s Feedback Loop at www.edn.com/article/CA6262536. Add your comments.

I/O module targets applications requiring high voltage

The new EPC182 from Micro/sys offers 64 lines of isolated inputs that can handle 3 to 50V dc and 16 relays for isolated I/O signaling with a switching capacity of 2A. A user-selectable pullup/pulldown resistor allows designers to pull each input high or low to ensure a known logic level at power-up. With a temperature range of −40 to +85°C, the EPC182 also fits applications that require high-voltage relay switching with interchannel isolation between the input signals.

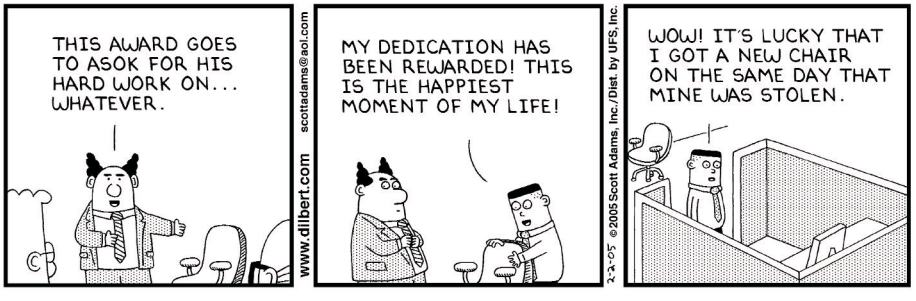
The board provides 16 lines with 1.5-kV-ac isolation using Form C relays. The board operates from a single 5V supply and typically draws 330 mA and 1.5A maximum. The EPC182 measures 4.53×6.5×0.6 in. and complies with the recently introduced EPIC (Embedded Platform for Industrial Computing) form factor. The EPC182 costs $375 (one).—by Warren Webb

▶**Micro/sys Inc,** www.embeddedsys.com.



The EPC182 I/O card offers PC/104 users 64 lines of isolated inputs plus 16 relays for high-voltage signal switching.

DILBERT *By Scott Adams*



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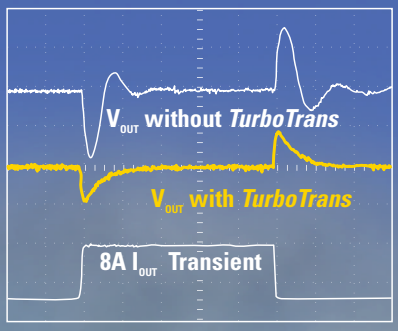
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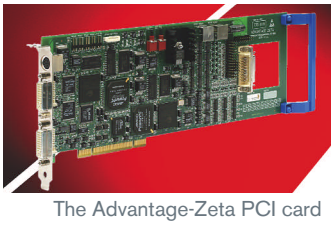
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Card integrates signal acquisition, scan conversion

Curtiss-Wright Controls Embedded Computing has announced Advantage-Zeta, a new radar-scan converter that combines signal acquisition and scan conversion onto a single PCI card. The card supports as many as three analog-video inputs and as many as eight digital-radar inputs. Advantage-Zeta digitizes and processes radar video and turning data for presentation to the radar-scan converter. The scan converter creates one or more plan-position-indicator views of the radar video, providing a display with resolution as high as 1600×1200 pixels.



The Advantage-Zeta PCI card combines radar-signal acquisition and scan conversion in a single slot.

The scan converter next combines the resulting radar picture with a graphics signal from any industry-standard DVI-compatible graphics card. The DVI output from the graphics card becomes an input to Advantage-Zeta, which intelligently mixes the radar-video picture with the incoming graphics picture to create a composite, multilayer display of overlay and underlay graphics. The card supports range correlation, enabling it to sample radar video at speeds as high as 50 MHz and reduce the samples to a programmed return length of 2048 or 4096 samples. The card supports radar-pulse-repetition frequencies as high as 8 kHz with optional azimuth correlation to reduce the output data to either 2048 or 4096 azimuths per scan.

Software support for Advantage-Zeta includes drivers for the Windows, Solaris, and Linux operating environments. Prices for the card start at $8500 (one).

—by Warren Webb

▷**Curtiss-Wright Controls Embedded Computing**, www.cwcembedded.com.

How low can 32 bits go?

11.21.05

With the new LPC2101, LPC2102, and LPC2103 microcontrollers, Philips Electronics continues to push down the lower limit for the price of 32-bit units. These ARM-7 TDMI-S-based devices sell for as little as $1.47 (10,000). Philips accomplished this lower price in part by offering on-chip memories as small as 2 kbytes of SRAM and 8 kbytes of flash. The other two microcontrollers offer as much as 8 kbytes of SRAM and 32 kbytes of flash. These devices will be available this month.

These devices improve on Philips' offering last year of less-than-$3 32-bit devices by increasing the clock rate from 60 to 70 MHz and maintaining no-wait-state operation from flash and SRAM. These devices introduce and implement fast, general-purpose I/O through the local bus that provides a fourfold performance increase in the ARM-7's bit-banging, so that it can support a 17.5-MHz toggle rate. All three devices include an eight-channel, 10-bit ADC that samples at 400k samples/sec.

These devices support expanded power management to enable designers to reduce power consumption to as low as 5 µA. Power consumption in power-down mode with the real-time clock running is less than 10 µA. The devices have as many as 32 5V-tolerant general-purpose I/O pins. Evaluation kits are available with prices starting at $99. The IAR Systems (www.iar.com) Kickstart kits include a free 32-kbyte compiler, and Keil Software (www.keil.com) evaluation kits include a free, 16-kbyte compiler.—**by Robert Cravotta**

▶**Philips Electronics**, www.semiconductors.philips.com.

FEEDBACK LOOP

"Americans seem to get in all sorts of knots with metric measures! As someone who started school learning imperial units and finished fully metric, I am glad I don't have to attempt engineering calculations using feet/inches/fractions, pounds/pounds-force/slugs, and arbitrary conversion factors!"

David Leske in *EDN*'s Feedback Loop at www.edn.com/article/CA6275409. Add your comments.

Kits speed video development

Xilinx's MVI (multimedia/video/imaging) systems are the first in a series on the XtremeDSP road map. The first product offerings comprise the VSK-4VSX35 video-starter kit, the XEVM642 video-coprocessing-development kit, and the new MPEG-4 encoder and decoder IP (intellectual-property) cores. The Xilinx VSK-4VSX35 kit targets video systems, and it comprises the ML402-SX35 development board and video-I/O daughtercard, a CMOS image-sensor camera, cables and power adapters, and reference designs. Xilinx's System Generator for DSP- and FPGA-design tools supports development. It also supports the DVI (digital-video interface), component-video and S-video interfaces, and the SDI (serial-digital interface).

The Xilinx video-coprocessing-kit daughtercard accelerates signal processing for the Texas Instruments DM642 EVM platform. The Xilinx Virtex-4 SX35 (VSK-4VSX35) video-starter kit and XEVM642 video-coprocessing-development kit will be available this month for $1495 and $1995, respectively. The MPEG-4 Part 2 encoder/decoder cores can handle scalable resolutions as high as D1—720×486 pixels—at 30 frames/sec. The Xilinx MPEG-4 IP cores are available now; prices are $20,000 for the decoder and $25,000 for the encoder.**—by Robert Cravotta**

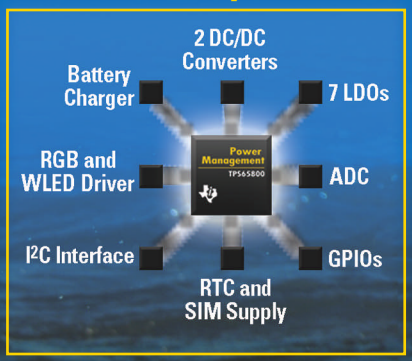
▶**Xilinx**, www.xilinx.com/dsp.

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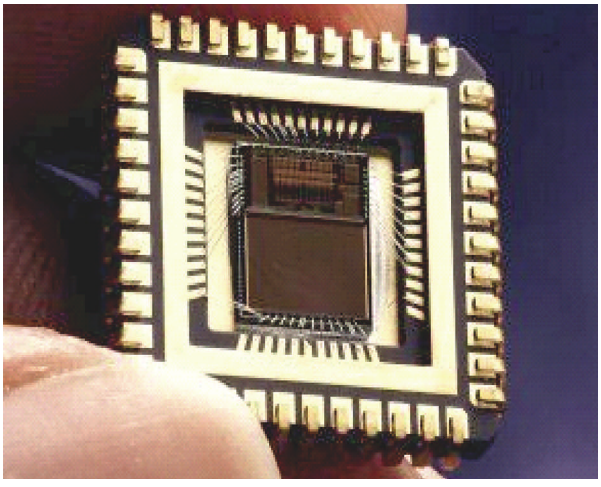
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GLOBAL DESIGNER

Imagers pose complex design challenges

Mobile-phone cameras are beginning to rival stand-alone digital cameras in resolution, and it won't be long before they will be able to shoot MPEG-4 videos and incorporate advanced algorithms for sophisticated manipulation of images. The insatiable demand for Web cameras, digital cameras, and mobile phones is powering a quiet revolution in the design and development of image sensors for mobile devices, according to Vivek Sharma, director of the India Design Center of STMicroelectronics.

"The main challenge is to control the power consumption of the image-signal processor, because battery power is at a premium in mobile-system applications," he says. "We also need to keep the chip small, because the board space in a mobile phone is at a premium. This constraint makes the interconnect routing a challenging task." ST India has recently designed a CMOS-imager SOC (system on chip) for mobile-phone applications. The work performed in India includes development of IP (intellectual-property) blocks, integrating and verifying the SOC, prototyping, implementing the RTL through GDSII (graphics-design system II) blocks, and developing firmware.

KS Raghunathan, head of the India Design Centre for Insilica Semiconductors, says, "Processing moving images and video at higher frame rates and sizes, implementing nonmechanical optical-zoom functions, increasing pixel count, and keeping costs reasonable are the main objectives." Although most Indian designers focus on CMOS imagers, Sarnoff Corp specializes in high-end CCD devices. Sarnoff's target markets for CCD and CMOS imagers are scientific, automotive, military, and semiconductor-inspection applications. These applications include spectroscopy, microscopy, and military applications that encompass both high-speed and low-light imaging. "We have been working on improving the process technology to reduce power consumption, improve frame rates, and increase manufacturing yield," says Vinayak Agrawal, lead design engineer at Sarnoff. The company also recently started working on reducing the noise in CMOS-imager circuits to a level comparable to medium-end CCDs and thus cut costs for applications that have traditionally employed CCDs.

—by Chitra Giridhar, *EDN Asia*

▷**STMicroelectronics**, www.st.com.
▷**Insilica Semiconductors**, www.insilica.com.
▷**Sarnoff Corp**, www.sarnoff.com.

BITS AND PIECES

Beijing-based Digital TransVideo Technology Co Ltd recently unveiled the DMD2000 plus and DMD3000 plus H.264 IPTV (Internet Protocol-TV) set-top-box digital-media devices, which target the IPTV market in North America. For more, see www.edn.com/051121p1.

Modbus IDA, ITEI open joint test laboratory

Modbus IDA, an organization comprising automation-device users and suppliers focused on the adoption of the Modbus-protocol suite, and the ITEI (Instrumentation Technology and Economy Institute) have opened the ITEI's Modbus Conformance Test Laboratory. The lab will test and certify automation devices that conform to the Modbus TCP/IP (Transfer Control Protocol/Internet Protocol) or Modbus-over-serial-line specifications. Modbus IDA will post tested devices on its Web site. "There is a lot of interest in China in the Modbus protocol and in the conformance testing of products to ensure that they comply," says Ken Crater, Modbus IDA president.

The lab is now testing devices in Beijing, and Crater believes that interest in Modbus will grow throughout China. The Standard Association of China has adopted three Modbus protocols that will find use in January in industrial automation. "The primary factor in the protocol is the vast quantity of available Modbus devices, such as I/O blocks, system controllers, and special-purpose devices," says Crater. "It has also long been a favorite of system integrators doing custom products, because it is easy to implement and custom-design."

—by Jeff Berman

▶**Modbus IDA,** www.modbus-ida.org.
▶**Instrumentation Technology and Economy Institute,** www.itei.cn.

11.21.05

R A Q ' s

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Check the Bias Current (Or How to Ensure that a Blessing is Heard)

Q. *The bias current in modern amplifiers is very small. Do I need to bother about it?*

A. At Mass in Limerick, Ireland (the location of one of Analog Devices' manufacturing facilities) one Sunday, the priest was rather softly spoken. Almost whispering into the microphone he said, "The Lord be with you." Nothing at all came out of the PA system and only the front row could possibly have heard him. Picking up the microphone he murmured to himself, "There's something wrong with the microphone." This was amplified to fill the church and the congregation responded to a man, "And also with you!" I restrained my mirth with difficulty and afterwards offered to fix the problem.



It was a moving coil microphone with a differential output to an SSM2019 preamplifier. The microphone was in perfect condition and delivering a signal to the amplifier inputs, but the connection from the cable screen to the metal microphone body was broken. A broken ground might cause hum (this barely happened), but why should it disable the amplifier?

When I examined the preamplifier circuit it became clear—the microphone's center-tap, which was grounded to the case of the microphone, carried the bias currents of the two SSM2019 inputs. With the ground open-circuited, there was nowhere for bias currents to flow and the amplifier stopped working. When Father Aidan touched the microphone, his body provided a current path to ground and everything worked again, albeit with a little hum.

All amplifying devices—bipolar transistors, JFETs, MOSFETs, and even tubes—have dc currents, known as bias currents, in their inputs. For some JFETs and MOSFETs these are as small as 20 fA (2E-14 amps)—about one electron every eight microseconds—but the inputs of op-amps and in-amps typically have bias currents in the range of pA to µA. A circuit design that does not accommodate these bias currents will not work properly, and may not work at all. But because they are so small, unintended leakage paths (the one through Father Aidan's body is an example) may often allow a badly designed circuit to work despite itself—but it probably won't work well. Good analog designs do not leave bias current effects to chance and good luck, but allow for them and ensure that they affect neither performance nor functionality.

Not only did I repair the broken connection, I also added two equal grounded resistors to the amplifier inputs ensuring that future microphone ground faults might cause hum but would not silence Father Aidan.

To learn more about how bias current affects op amps,
Go to:
http://rbi.ims.ca/4401-501



Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

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Freescale's Sam Coursen:
It takes one to know one

Sam Coursen is the chief information officer at Freescale Semiconductor. These days, that title usually goes to people with degrees in computer science or master's degrees in business administration. But Coursen is different. When he graduated from Auburn University (Auburn, AL) in 1973 with a bachelor's degree in electrical engineering, chief executive officers and computer-science degrees didn't exist. Before joining Freescale, Coursen, a Georgia native, spent seven years at NCR and 23 years at AT&T.

How much of an advantage is it being an EE while working at a semiconductor company?

A What's important is to understand how chips are manufactured at each station. You have to understand at a high level how to design a chip to provide the systems that support them. I don't have to go that far down in the process. As a chief information officer, you also have to do two things at once: You have to run networks and engineer the IT function. Simultaneously, IT is trying to add value to everyone's process. IT is both a process and an enabler of all the other processes. The chief information officer has to know enough about the other processes to deliver solutions.

Were you ever a designer?

A I have a long history of software development at the OS and application levels. These days, you have to do both software and hardware. We have to understand what those applications do to make the hardware designers more productive.

How unusual is a chief information officer with an EE background?

A It's not too unusual. More recently, they are from computer-science backgrounds, but when I graduated from college, most schools did not have computer-science programs. You were in EE.

What's different about being in a semiconductor company from others you've worked for?

A Fab manufacturing is unique, and that's the major difference. The business is more cyclical than in my past jobs. At first, I had to put on a white suit and go through the plants to understand how the systems are supported.

How would you describe the systems?

A There's the ERP [enterprise-resource-planning] system on the front end that sends orders down to manufacturing. All the equipment stations are on the LAN. We download instructions into the equipment, which is always measuring. We have to understand the



performance of the factory and equipment usage to get the IT systems aligned with how the process works. If you provide the right systems, you find out when the equipment is getting out of spec, so you avoid downtime or producing bad chips that you have to throw away. You learn how productive the labor in the factory can be.

All of these steps produce lots of data that is critical if you're trying to figure out why a customer returned a part and why it is failing. It might be an equipment setting. One important thing is pulling the data into a central database to make that analysis easy to do. One of the key initiatives is making it easier for technicians to get their hands on all this different data.

What is your return rate, and what are you striving for?

A There's a separate scorecard for each customer. We are providing tools to keep improving those numbers. You don't get 100%. We are trying to raise not only the quality, but also the yield. Higher yields translate into profit.

What has surprised you the most about Freescale so far?

A I had done a lot of research, so nothing was a big surprise. It's a company with a lot of tradition, but, at the same time, it feels like a start-up. It's a little bit the best of both worlds. We want to be nimble and aggressive, and sometimes you don't find those characteristics. I worked for AT&T when we had a million employees. It was well-managed from a quality standpoint but was not built to react quickly to things. It wasn't a 'get-your-juices-flowing' type of thing.

Why did you choose electrical engineering?

A My family has a strong aptitude for science and mathematics that leads to engineering as a field of study. My three sons are studying engineering, and the oldest is in computer engineering. One is a junior studying electrical engineering at Ohio State, and the one in high school says he will pursue it, too.

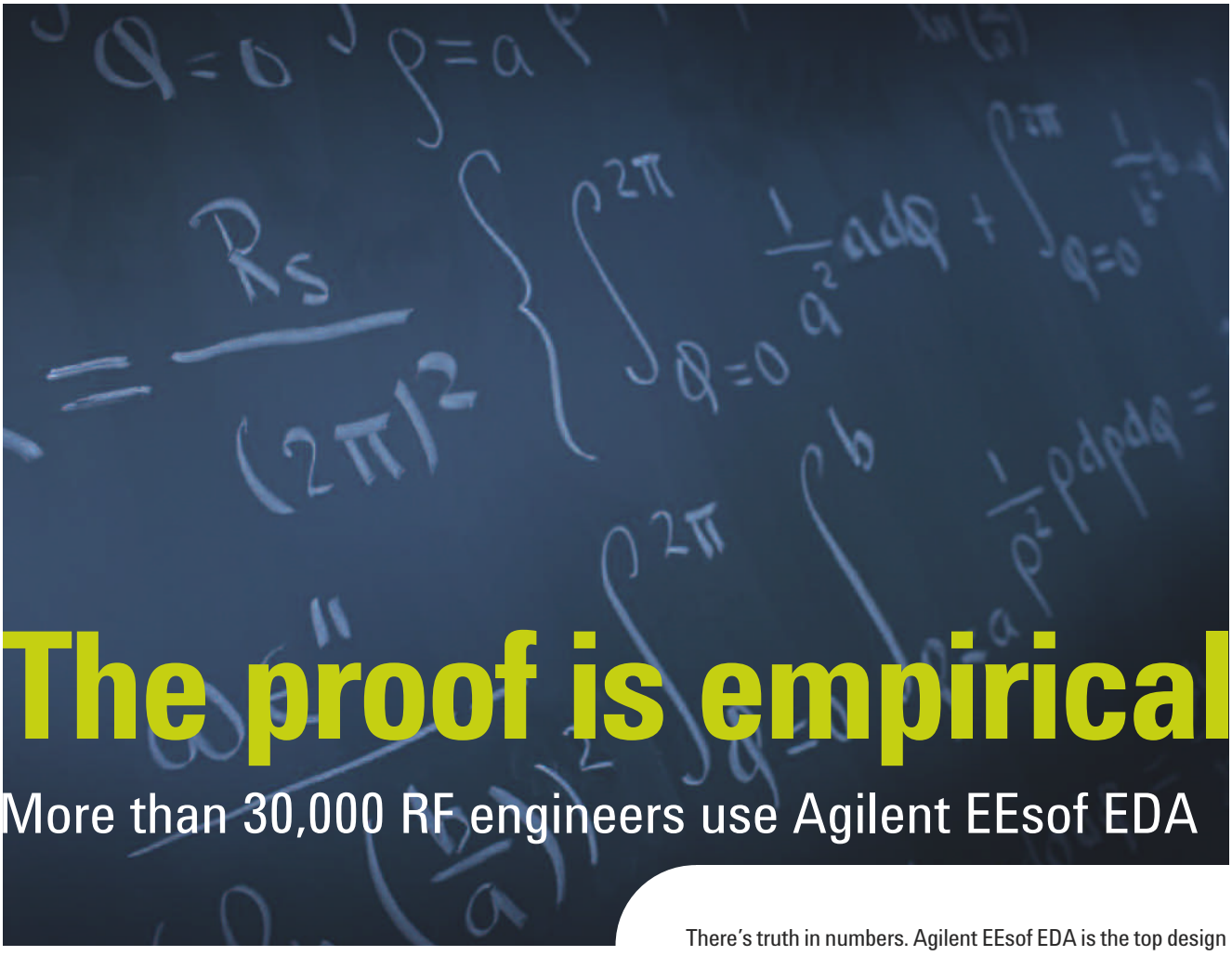
How concerned are you that the ranks of EEs are thinning?

A I worry, and yet I don't. If you go back a few years, Japan was going to take over everything. It took over things that were very repetitive, but it did not take over innovation. We need to play on our strength, which is innovation. That's what the United States does well. We need graduating engineers to spur that innovation.

How do you network with colleagues?

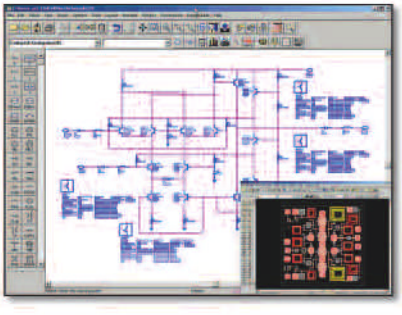
A We're reaching around the technical community and creating linkages. I've started a relationship with the University of Texas and asked whether they're interested in having me on their advisory board for the engineering school. It's important to get involved.

—by John Dodge,
Editor in chief,
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BY BONNIE BAKER

Protect your circuits from ESD occurrences

Oh, the things they don't teach you in college. In my first week of employment, I wore leather-soled shoes and nice polyester slacks. So dressed, I picked up a customer-returned JFET operational amplifier and plugged it into a test socket. The part was dead. Overcoming discouragement, I inserted a second customer op amp into the test socket. The second part didn't work, either. I didn't see any sparks, but I had successfully destroyed two amplifiers before they even got into the socket. Simply walking across a vinyl floor can generate thousands of volts at your finger tips. In sunny Arizona, you can easily generate an average of 12 kV, with 20% relative humidity (**Figure 1**).

The most prevalent ESD damage that you can inflict on MOS devices is oxide punch-through. Oxide punch-through occurs when you expose the silicon to an extreme overvoltage condition that exceeds the chip's gate-oxide, dielectric breakdown voltage. The results of this condition can cause overheating and an eventual short. Junction and metallization burnout are secondary failure mechanisms. Failures due to junction burnout manifest themselves as high reverse leakages or as a total short; metallization burnout manifests itself as localized melting and an eventual short. ESD damage can also manifest itself as parametric degradation. This type of failure appears as a latent failure.

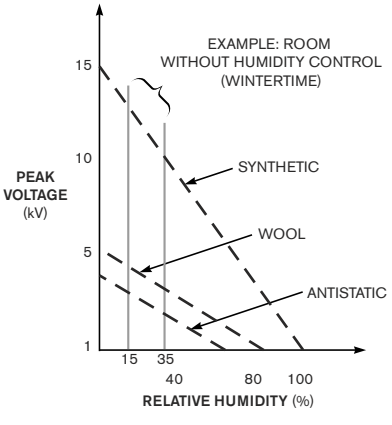


Figure 1 The maximum value of ESD voltages depends on the relative-humidity percentage and the clothes you are wearing.

People are the largest source of static. They carry static in their clothing and come in contact with static charge in their environment. IC manufacturers provide a first line of defense, with on-chip protection devices that can withstand ≥2-kV (human-body-model) ESD events. Additionally, you can control the static electricity in your environment with prevention. Grounded wrist straps, static-dissipative table tops, conductive heel straps, and grounded floor mats provide a good second line of defense. ESD awareness and education in your work area can also reduce the risk of damaging sensitive devices.

Unprotected chips on a pc board are equally vulnerable. They show their vulnerability at the I/O ports of a controller; at the RS-485 socket; at the Ethernet receivers; and at any hot-swap interface, such as a USB port. Portable devices are adding functions and increasing their exposure to ESD or EFT (electrical-fast-transient) events. EFT is a result of the parasitic capacitance and inductance at an I/O connector or between the wires in the data cable. In most systems, wrapping power lines with data lines produces inductive-switching surges into the data lines. In all of these situations, the potential voltage difference between two unconnected terminals is an ESD or EFT event waiting to happen.

At the pc-board level, you need to design in precautions. As a high priority, you need to use good layout practices, such as ground planes, loop reduction, and antenna elimination in your traces across the board. Another good defensive measure is to use a transient-suppression device. This device should be able to clamp surge voltages to safe levels, respond to fast changes in voltages (dV/dt), and fit into small places on the pc board. The most effective transient-suppression device on the market is the TVS (transient-voltage-suppression) diode. The TVS diode has low capacitance, a subnanosecond response time, low clamping voltage, and the ability to withstand a 30-kV ESD incident (per the IEC6000-4-2 ESD standard). The best place for the TVS diode on your board is at the point of entry or at the edge of the board.

Should you always take ESD precautions? Yes. If you don't pay attention to ESD or EFT details, you may be evaluating a device or a pc board that an invisible spark long ago compromised. EDN

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Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.baker@microchip.com.*

Intersil Battery Charger ICs

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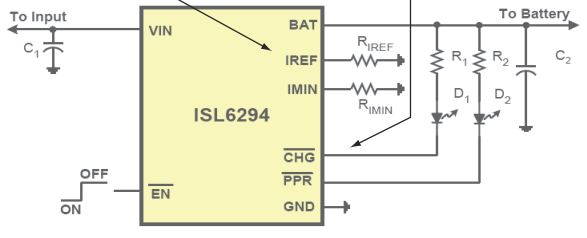
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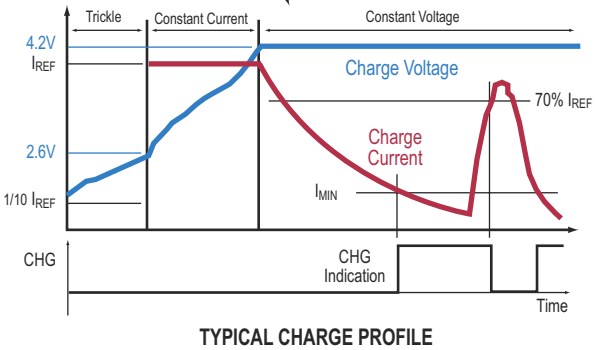


The constant current I_{REF} is set with the external resistor R_{IREF}. The constant voltage is fixed at 4.2V.

End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



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Driverless vehicles take on the desert

The Darpa Grand Challenge—not since the fabled transcontinental races of a century ago have so many engineers, professors, students, corporate teams, and garage tinkerers been drawn to so daunting a task. On the surface, it seems, well ... impossible. Once the race starts, the design teams can do nothing. There's no remote control, no driver. Using stereo cameras, radar, and lasers, the vehicles themselves must check for obstacles, then roll forward at speeds up to 60 mph, across sand dunes, through valleys, along highways, and over rivers, all the while obeying the way-points beamed to them from global-positioning satellites.

In behavior-based detection, computers employ logic to chart a vehicle's course. In the map-based method, a vehicle employs multiple sensors—stereo cameras, radar sensors, laser sensors, LIDAR (light-detecting-and-ranging) devices, or some combination of these items—in an effort to obtain different kinds of data to build the so-called "terrain map." Vehicle computers then employ home-grown software to examine the incoming data and identify potential obstacles. Virginia Tech University's "Rocky" vehicle, for example, creates a software grid resembling a tile floor, with grid spaces representing about one square foot. The vehicle's computer then examines incoming data from a Sick Optic laser measurement system and populates those software spaces with numbers ranging from 0 to 10, with tens depicting the worst kinds of untraversable obstacles.

Carnegie Mellon's vehicles ("Sandstorm" and "Highlander") carry Intel NetStructure servers that hold five so-called "blades," each with Pentium M microprocessors. The Pentium Ms handle sensor data, planning tasks, and action tasks, such as signaling the drive-by-wire units that propel, steer, and brake the vehicle. Carnegie Mellon's vehicles also use a smaller, rack-mount server that incorporates a parallel computing architecture. This architecture contains two Intel Itanium microprocessors that offer better floating-point operation than the Pentium M and take on the more compute-intensive task of turning sensor data into navigation information.

Extraordinary computing lengths will be increasingly necessary as vehicles drive faster; therefore, vehicle electronics will need to look farther out onto the horizon. Carnegie Mellon, for example, ultimately wants to look out as far as 50m ahead of the vehicle but can't do so yet because such measures would require more computing power.

Computing is an extraordinary challenge because it must serve as the underlying foundation for two functions: following the GPS way-points and avoiding obstacles on the course. Way-point following in itself can be difficult, entrants say, and it can become more so when finicky GPS units fail to send ground data. Then, they say the vehicles must use an inertial navigation system (INS), consisting of a combination of gyroscopes and accelerometers, to determine where they are. The INS accomplishes that task by using the accelerometers to provide acceleration information in three axes and the gyroscopes to supply angular velocities.

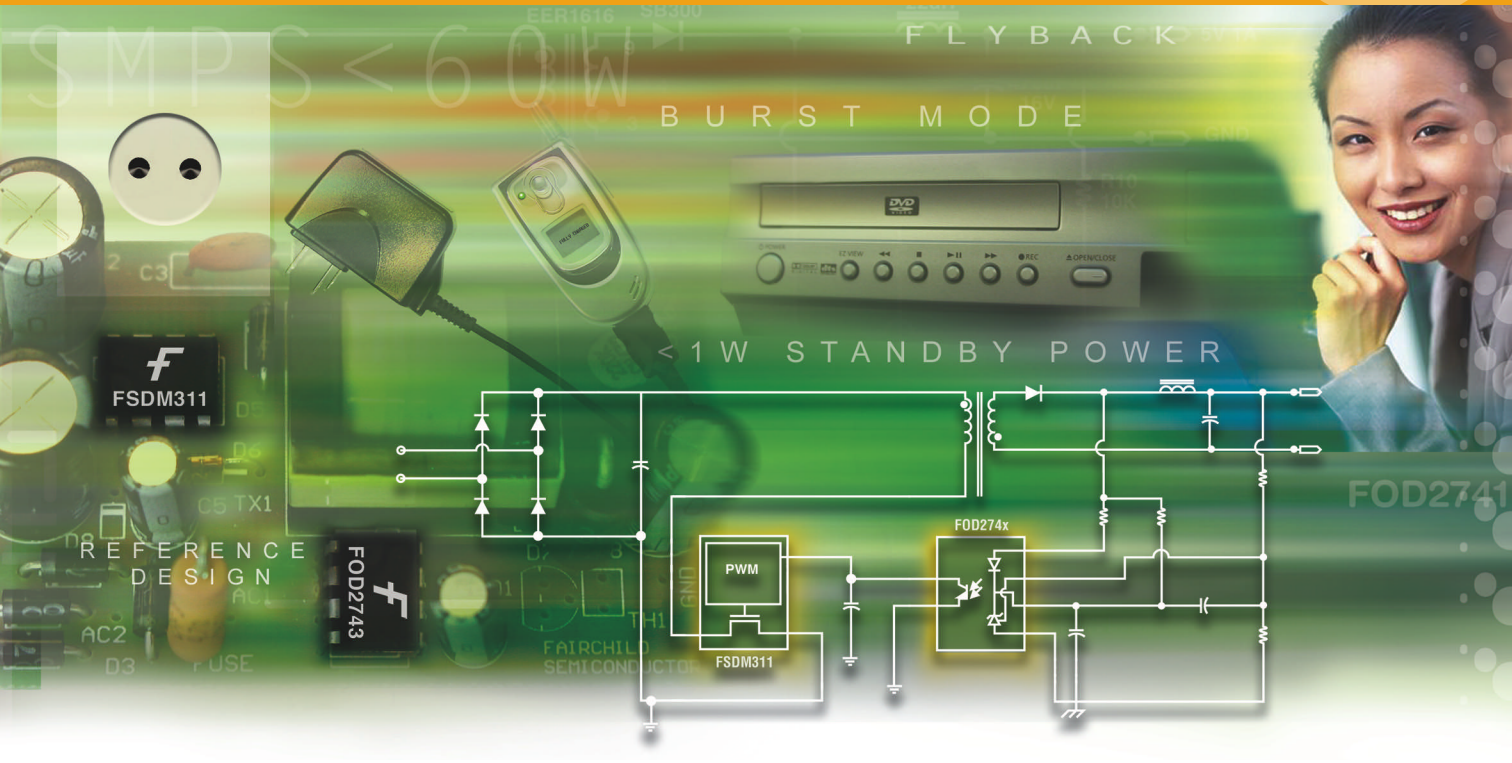


DAVID SHARPE

After no vehicles completed the Grand Challenge course in 2004, 23 vehicles attempted the feat on Oct 8, 2005. Faced with traversing a 132-mile course through the Nevada desert and finishing in the shortest elapsed time under a 10-hour limit, five teams succeeded. Stanford University's "Stanley" vehicle took top honors, finishing in 6 hours and 53 minutes. For details on the course, contestants, and results, check out www.grandchallenge.org/.

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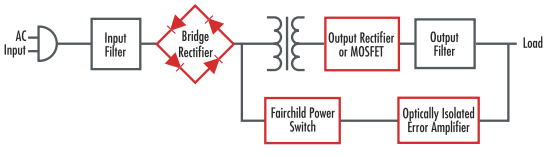
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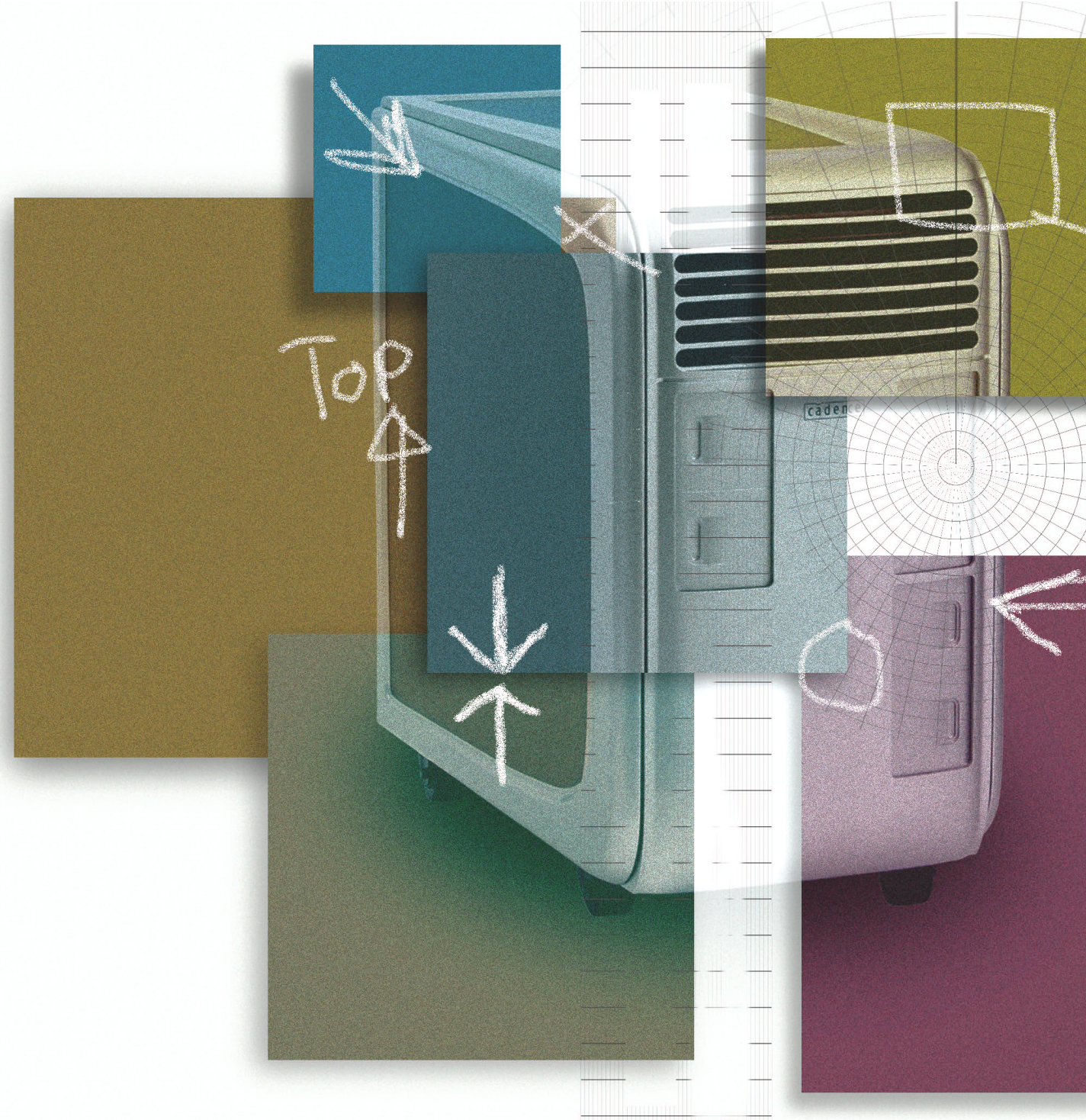
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BY MICHAEL SANTARINI • SENIOR EDITOR

ASIC PROTOTYPING: MAKE

AS DIGITAL-IC DESIGNS HAVE BECOME MORE COMPLEX, SO TOO, HAS THE TASK OF VERIFYING THEIR FUNCTIONS. OVER THE YEARS, EDA VENDORS HAVE DONE LITTLE TO REDUCE THE GAP BETWEEN THE NUMBER OF GATES YOU CAN DESIGN AND THE NUMBER YOU CAN VERIFY IN A REASONABLE AMOUNT OF TIME.

IC designers often spend as much as 60 to 80% of their time simply verifying designs, and that percentage is growing. To get a leg up on verification, many design groups have turned to hardware-assisted verification to prototype their designs. Breadboarding was the first form of hardware prototyping, and it has since grown in sophistication and popularity. Studies from Collett International (www.collett.com) and Deepchip.com (www.deepchip.com) suggest that 30 to 40% of all ASIC projects involve prototyping. You can now build your own multimillion-gate prototype using off-the-shelf FPGAs, but, for large or complex designs, you may want to buy predesigned prototyping systems or, if you can afford it, rent or buy a simulation accelerator or an in-circuit emulator. The decision to build, rent, or buy depends on several factors, including required clock speed, capacity, functions, cost, system-design skills, and the time you have to verify your design (**Reference 1**).

PROTOTYPING SYSTEMS

Prototyping ASICs and SOCs (systems on chips), say designers and vendors, is essentially a step backward—turning an SOC into what some refer to half-jokingly as an SOB (system on board). In building a prototyping system, some designers reconstruct the functions of their ASICs using a mixture of discrete components, legacy ASICs, and FPGAs providing new functions. Others construct or even buy a fast-prototyping system in which the design is programmed into a motherboard. The motherboard holds an array of FPGAs and daughterboards to connect to unique functions or a larger system.

Engineers can design or buy an ASIC-prototyping system that runs at speeds approaching 250 MHz—a performance level that in some cases approaches the speed at which the final chip will operate. Such a prototyping system is much faster than commercial emu-

VERSUS BUY

AT A GLANCE

- Acceleration is 10 to 50 times faster than RTL simulation.
- Emulation is 1000 to 5000 times faster than RTL simulation.
- FPGA prototypes can be 10,000 times faster than RTL simulation.
- EDA vendors now offer partitioning software that simplifies building prototypes.
- Multiple vendors offer FPGA-prototyping boards for less money than it would take you to build your own.

lators that top out at 2 MHz and 110 times faster than an RTL simulator. Designers can use fast-ASIC-prototyping systems to test the functions of the design in the system environment or to get a jump on embedded-software development.

The drawback of ASIC prototypes, however, is that they are harder to debug because it is difficult for designers to pinpoint the exact location of a bug on these systems. Design groups base their prototypes on extensive simulation-based verification. MIPS Technologies uses almost every form of hardware-based acceleration to verify new microprocessor-core designs and to help customers integrate cores (see **sidebar** "MIPS uses it all").

ROLL YOUR OWN

Building a prototyping system from scratch is now in some ways easier and in other ways harder to do than it was in the past. The huge capacity and speed grades of today's FPGAs allow users to prototype multimillion-gate ASIC designs. In recent years, EDA companies such as Synplicity and Synopsys have eased prototyping tasks by offering tools to help engineers partition ASIC designs and program their partition blocks into arrays of FPGAs. Today, commercial availability of ASIC-prototyping software has invigorated the fast-prototyping business and made it a more formidable competitor to traditional emulation vendors, such as Cadence Design Systems and Mentor Graphics. Vendors, especially those offering off-the-shelf prototyping systems, say that the big question for those considering making or buying a prototype is: Do you have the time, the extra engineering staff with the pc-board- and system-design skills, and the budget to build a prototyping system on your own?

Mike Dini, president of The Dini Group ASIC-prototyping company, strongly suggests that it is cheaper to buy a fast prototype than to build one from scratch. Dini 10 years ago was an ASIC- and FPGA-design consultant, and, because he needed verification tools, he started building prototyping boards. He has now dropped the design-services gig for what has turned into a booming business in ASIC prototyping. Multiple vendors now offer such prototyping systems (**Table 1**). "Our competitors in emulation say we simply offer a bucket of FPGAs,"

TABLE 1 FAST-PROTOTYPING-SYSTEM, ACCELERATOR, AND EMULATOR VENDORS

Company	System	Type	FPGA or custom processor	No. of ASIC gates	Built-in software (partitioning, debugging)
Cadence Design Systems	Xtreme Series	Accelerator/ emulator	FPGA with reconfigurable-computing coprocessors	4 million to 50 million	Partitioning and debugging software
	Palladium Series	Accelerator/ emulator	Custom ASIC processor based	4 million to 256 million	Partitioning and debugging software
The Dini Group	DN8000k10	Prototyping system	Virtex-4 FPGA based	1.5 million to 24 million	None, must use Synplicity
EVE	ZeBu (Zero Bugs)	Emulator	Virtex-4 FPGA based	750,000 to 6 million for PCI-card-based system or 48 million for box	Automated partitioning and debugging
Flexody	FlexCube	Prototyping system	Virtex-4 FPGAs	1 million to 18 million	ARPcom
Gidel	Processor board and tools	Emulator and prototyping systems	Stratix II FPGAs	60,000 to 20 million	Simulation acceleration, hardware/software integration, debugging
Hardi Electronics	HAPS (ASIC-prototyping system)	Prototyping system	Virtex-4 FPGAs	3 million to more than 30 million	Self-test, no configuration necessary
Mentor Graphics	VStationPro	Hardware emulator	FPGA	1.6 million to 60 million	Fully automated compilation, fully integrated debugging capability
ProDesign Electronics	Chipit (silver, gold, platinum)	Prototyping system	Virtex-4, -2, and -Pro FPGA based	30,000 to 20 million	Yes
Tharas Systems	Hammer S-Class	Accelerator/ emulator	Multicore custom processor	8 million to 16 million	Compiler for Verilog and VHDL
	Hammer M-Class	Accelerator/ emulator	Multicore custom processor	32 million to 256 million	Compiler for Verilog and VHDL

says Dini. "I don't take that as an insult. That's exactly what I do. I put a bucket of the most humongous FPGAs on a board, put it together for you, debug it, and sell it to you for cheaper than you can build it on your own." He says that prototyping can be invaluable, but putting together an application-specific board that you'll likely end up throwing away after the project is finished can be wasteful. He suggests that users create daughtercards of their specialized functions and purchase the FPGA part of the prototyping system from a fast-prototyping vendor (see **sidebar** "The case for buying" at the Web version of this article at www.edn.com/051121cs).

Dini and others say that, even with automated partition software from companies such as Synplicity and Synopsys, building a system on your own with more than three FPGAs can quickly become a nightmare, especially if you are unfamiliar with pc-board design, which, despite what EDA vendors claim, is still a tough task. "Prototyping is a make-versus-buy decision," says Dini. "With bigger packages that have 700 pins, putting one Virtex FPGA on a board is OK, but putting two, three, or 16 becomes difficult to design, build, and test. For example, two 700-pin FPGAs are too much for pc-board autorouters, so a lot of manual work has to go into it. The pain threshold, at which homegrown FPGA-based ASIC prototyping becomes complex, is around three. Two is not bad, but when you get to implementing three FPGAs, you have to start looking at layer counts and how things connect in the pc board," he says. He points out that modern FPGAs are well-suited for automatic-partitioning software and that most fast-prototyping vendors tailor their systems to work with Certify from Synplicity, for example.

Dini says that the latest FPGAs tout advantages in I/O structure, rather than speed or logic. They integrate serializers/deserializers that connect with differential pairs, so if you connect one FPGA to another FPGA, you need a differential pair operating at approximately 350 MHz

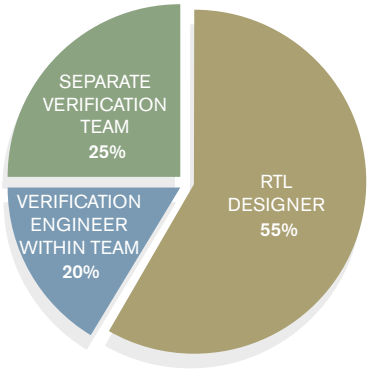


Figure 1 A verification team that is unfamiliar with the ASIC design typically does prototyping (courtesy Synplicity).

with 10-to-1 multiplexing. If your design operates at 35 MHz, you can get 10-to-1 multiplexing on 108 pairs with 1800 signals partitioned between two FPGAs. "That approach dramatically eases the partitioning task, which is a nightmare in homegrown systems," Dini says. One way

(continued on pg 36)

Price per gate	Starting price	Price of fully loaded system	Rental available	Architecture
Starts at $0.036	$144,000, including maintenance	$6 million for multiuser, 50 million-gate system; $3 million for single-user, 50 million-gate system	Perpetual license or time-based license	Event-based
Starts at $0.072	$288,000, including maintenance	$38 million for 256 million-gate Palladium II, $15.4 million for 128 million-gate Palladium I	Perpetual license or time-based license	Cycle-based, scheduled
Less than $0.01	$11,000	$135,000	No	Cycle-based
$0.02	$25,000	$300,000	Yes	Both
$0.03	$120,000	$440,000	Rent or buy	NA
Less than $0.01	$1345	$140,000	Buy	Cycle-based to free clock
$0.01	$9000	$69,900	No	Both
$0.09	$450,000	$5.7 million	Yes	NA
$0.01 to $0.02	$10,000	Less than $500,000	No	Cycle-based
$0.03	$250,000	$525,000 to $925,000	Six-month minimum rental, perpetual license, or subscription	Event-based
$0.06	$1 million	$1.275 million to $1.875 million	Six-month minimum rental, perpetual license, or subscription	Event-based

MIPS USES IT ALL

Microprocessor-core vendor MIPS Technologies uses several forms of hardware-assisted verification to develop its cores. Donald Ramsey, director of CAD and information systems at MIPS, says that his group uses Mentor Graphics' VStation emulators and also builds its own prototyping boards for verification and for customers. Its processor cores have 500,000 to 1 million gates, so capacity is not an issue for running the core in either emulation or single-FPGA prototyping boards.

"We don't have a gate challenge, but we do have a complexity challenge in that the corner cases of general processor are deep, and the design requires an immense amount of directed testing, pseudorandom testing, and then prototyping and emulation as a verification vehicle, a debugging vehicle, and for software verification," says Ramsey. "When we create a core, we expect a number of software tools to work, as well."

Microprocessor-core design starts with RTL simulation on computer farms. The company then uses emulation upfront in the process. It has two VStation emulators and uses one for functional verification and the other, which connects to the system, for in-circuit emulation for debugging. For verification, the team uses emulation as a simulation accelerator for a fast, directed, random verification. "We get about a billion cycles a day out of our emulator," he says. "It is just like having a faster simulation engine."

MIPS uses another VStation for system-level simulation. "We can't run applications on our RTL simulator, partly because it is too slow and because, in a system environment, you have to abstract things because it is not just a core; it needs system controllers, memory, and all that," he says. "Then you run into a gate-count issue."

Rather than test the RTL version of the core for in-system testing, MIPS loads the design onto an emulator. Before using emulation, MIPS design groups used a previously developed prototyping board for internal software developers to get a head start on embedded-software development. "It was basically a pc board with an AT form factor and PCI slots that allow you to connect disk drives, keyboards, and the like. Instead of a processor, the system had a daughtercard with two slots—one for an FPGA to program a system controller and another to place a MIPS processor," Ramsey says.

MIPS then created a new daughtercard that would allow the company to plug the emulator into the FPGA-prototyping system and perform in-depth system debugging. MIPS also directly programs the processor design into the FPGA on the daughtercard. FPGA prototyping runs faster than the in-circuit method and identifies bugs but lacks the in-depth visibility into the code. Whereas the FPGA prototype runs at 25 to 40 MHz, the system with emulation runs at 1 to 3 MHz. This speed requires users to do an excessive amount of clock buffering to account for naturally occurring wait states in memory and hard-coded interval timers in an operating system, Ramsey says. An FPGA prototype is eight to 12 times slower than the actual processor and is better for debugging.

WHEN YOU STEP DOWN FROM 25 TO 1 MHz, YOU'VE STEPPED OUT OF THE BOUNDS OF WHAT A REAL SYSTEM LOOKS LIKE.

Many memory subsystems can tolerate that factor of eight- to 12-times speed decrease. "When you run the FPGA, it has all the characteristics of a normal system, but it just runs a bit slower," Ramsey says. "But when you step down from 25 to 1 MHz, you've stepped out of the bounds of what a real system looks like. Even if you have a slow memory on the board, it looks like you return data on the next cycle. You have to be careful because you are really not modeling all the wait states in a real system because the memory and other peripherals are always available."

According to Ramsey, designers can also encounter issues with hard-coded interval timers in an OS. "You have to do some time-scaling, too," he says. Because of a shorter development cycle, MIPS used emulation and FPGA prototypes for hardware debugging on its last design. "We would run things on the emulator, quickly find a lot of issues, and then found that we needed a faster platform if we're going to meet schedule. The team then decided to use an FPGA prototype. It took a few minutes, rather than one to three hours, to find the OS bug."

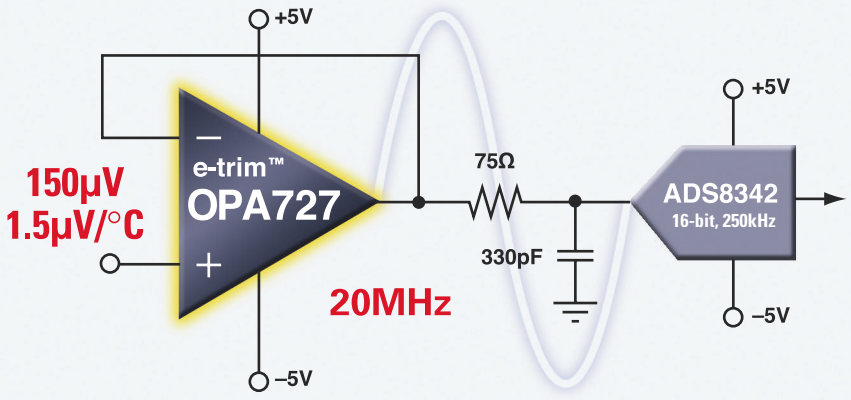
Once the team found the bug, he says, it had difficulty locating its source. "In an emulator, it was 100% visibility, but, with this emulation system, you don't have full history, so you have to trigger close to when you think the event was to capture the event. In the emulation, you wind up doing multiple runs to find your trigger point, and, once you do, you have the smoking gun," he says. "In an FPGA run, it is the opposite. You know where the trigger point is, but you run it until you get the correct set of signals out, and then you go back and write a directive diagnostic and run it on the simulator to validate your theory."

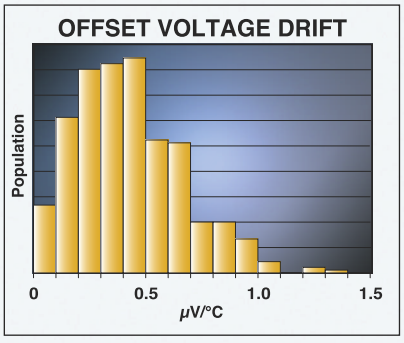
In some cases, it proved impossible to write directive diagnostics; it became difficult to pinpoint problems because of the differences between time interrupts, memory speeds, and processor speeds in a complex processor with a lot of outstanding operations. One of the legacy problems with emulation systems is that users had to spend as much time debugging the emulator as they did debugging their designs.

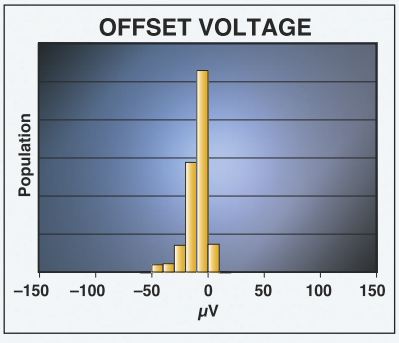
EDA vendors have made strides in facilitating emulation systems, and Ramsey's group did extra work to remove the kinks from the emulator.

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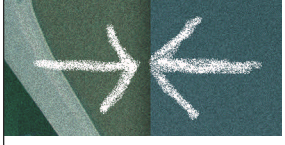
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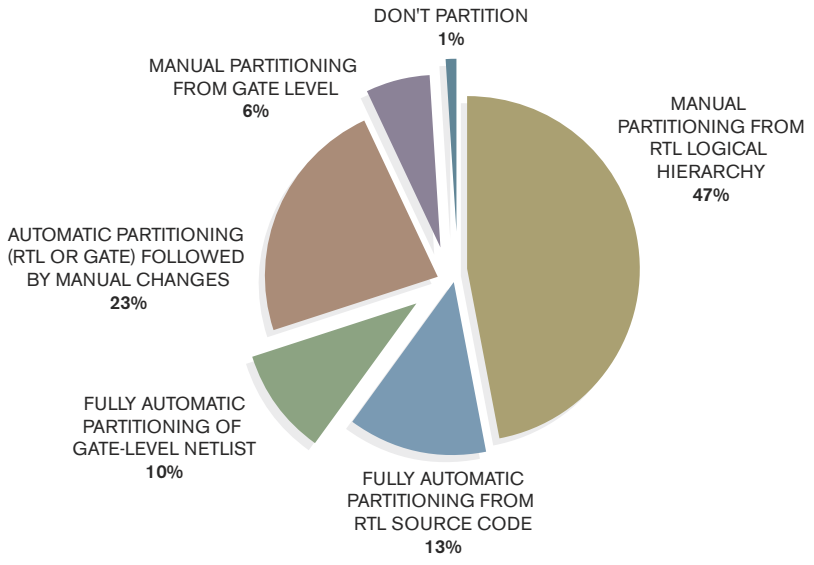


Figure 2 Even with automated partitioning software, programming an ASIC-prototyping system requires some manual partitioning (courtesy Synplicity).

to work ASIC prototyping into the design is to ensure before the design project that the ASIC developers design with prototyping in mind. Another approach is to arrange blocks in the ASIC to accommodate partitioning. Getting ASIC designers to buy into this idea is often difficult. "The ASIC designer is often the top of the food chain, however," he says. "Verification and prototype are on the bottom of the food chain, even though they shouldn't be."

John Gallagher, director of ASIC-tool marketing at Synplicity, says that the partitioning task is generally easier the more familiar you are with the ASIC design. A Synplicity study with 450 respondents from the design community shows that 55% of RTL designers are responsible for partitioning the ASIC into a prototyping system, but 25% say that a separate verification team does the prototyping (**figures 1** and **2**).

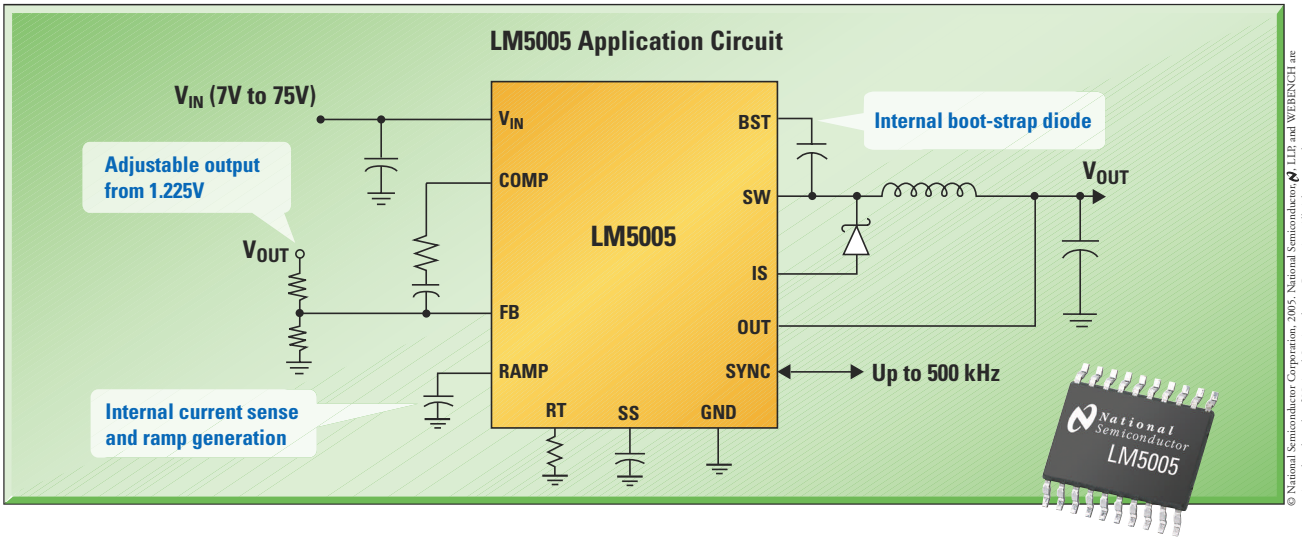
ACCELERATION AND EMULATION

Design groups wanting to maintain the verification visibility of simulation while also speeding verification can do so by using simulation acceleration or emulation. With acceleration, part of the design compiles and runs on the hardware accelerator. With emulation, the entire design runs on hardware. Acceleration runs code hundreds or even thousands of times faster than pure simulation running on workstations, but it is too slow to run a design in-circuit that connects to the rest of the system. Emulation, on the other hand, can be hundreds or even thousands of times faster than RTL simulation, and designers can streamline it to run at approximately 2 MHz, which allows its use in-circuit and as a way to speed functional verification. Designers can even tweak some systems, such as Cadence's Palladium emulator, to run at tens of megahertz, the company claims.

Vendors build acceleration and emulation systems with big, commercial FPGAs, much like prototyping systems, or with custom processors. Those offering systems with custom processors claim that the devices are faster and more efficient simply because their architectures are designed for acceleration and emulation, unlike systems using off-the-shelf FPGAs. ATI Senior Verification Engineer Art Stamness buys into the use of acceleration but not emulation. His group develops the 3-D-graphics cores in the company's graphics-processing units, and the group uses Tharas Systems' accelerator to verify designs. "We map a portion of our simulation testbench onto a hardware accelerator that uses custom processors," he says. "It gives us faster turnaround. Instead of running an FPGA netlist, we compile a binary, and that can run multiple magnitudes faster than doing the emulation." It can take a day just to compile a netlist

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with an emulator. "If you find a bug, you have to recompile, wait until the next day, and then, if you find another bug, you have to wait another day," he says. Acceleration, on the other hand, can find bugs and have another netlist ready for more tests within an hour.

Acceleration is much closer to a simulation environment, and it can take a lot of code you wouldn't otherwise feed into an emulator. And, acceleration provides a dramatic increase in performance over simulation but not the 5000-fold better performance that an emulator provides.

Stamness' group works with a 150- to 250-PC server farm running Cadence NC-Sim with the Tharas accelerator in cosimulation mode. The Tharas compiler extracts the sizable code and creates a "stub" for the design. NC-Sim runs on the host machine that communicates with the hardware accelerator. Stamness suggests that using emulation involves not just start-up costs, but also support costs. "The amount of support infrastructure in hardware, personal, power, and lab space required is prohibitively expensive compared with an accelerator, which drops into a rack like any simulator box and gives faster performance," he says. "Emulation still scares people and is reserved for the high end, where acceleration is in a good position to fill the space between the $1 million box and slow simulation."

EDA VENDORS SAY THAT THE SOFTWARE THAT UNDERLIES EMULATORS IS NOW MORE SOPHISTICATED AND EASIER TO USE, AND MUCH OF THE COST OF THE SYSTEM COMES FROM ITS EASE OF USE.

Stamness' views of emulation are typical of those who have invested in multimillion-dollar emulators only to find them gathering dust or obsolete some years later. Early emulators were difficult to program, and users often found themselves spending as much time debugging the emulator as the IC design. EDA vendors say that the software that underlies emulators is now more sophisticated and easier to use, and much of the cost of the system comes from its ease of use.

Tom Paulson, verification engineer at QLogic, is another emulation convert. His team uses Cadence's Palladium PD II emulator for building fiber-channel-switch ASICs. The company has for more than three years been using the Palladium emulator to verify five ASICs. The QLogic team came up to speed on Quick-turn emulation by using its QuickCycles

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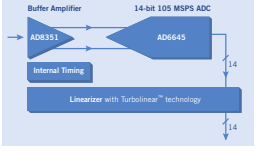
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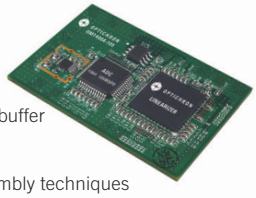
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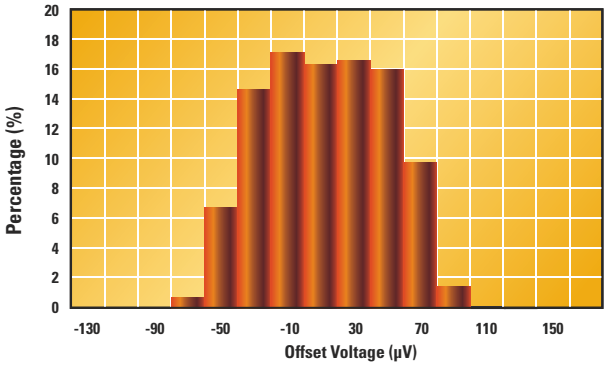


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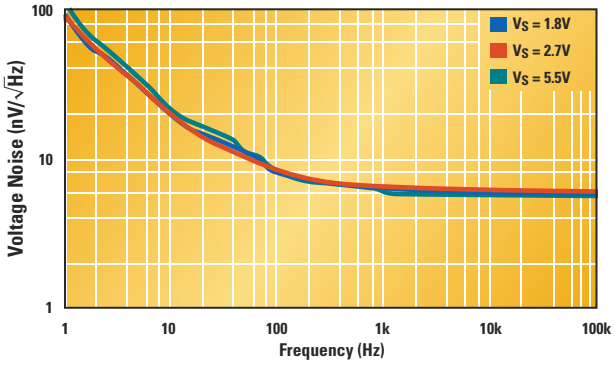
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rent-to-own program and then eventually purchased a box. "It cost a lot, but we've kept it busy," he says. Paulson's division works with VHDL and uses Mentor's MTI ModelSim for initial verification. "We automated the process, as you would expect with companies that do something over and over again," says Paulson. "We build a set of ROMs, and each test calls out a different ROM, so the chip would operate slightly differently. We run a test or may run four or five tests against a ROM. We set up those configurations with TCL [tool-control-language] scripts. The end result of all that checking is simple: With a fiber-optic chip, you are checking that everything got to where it was supposed to go, and you account for all the fiber-channel frames—that is, that all the frames arrived correctly. We also do some internal checking and check status registers within the chip. It's a pass/fail when you get to that point," he says.

If the team finds a bug, it reruns the test and then uploads the database to a workstation. The team then uses the debugging tool offline. "We have a certain amount of window we can view on a trace and a certain [number] of signals we can ask for in the beginning," Paulson says. The team is also starting to use Cadence's IXE 3.0 software, which reconstructs the design in software. "We are seeing remarkable increases in the amount of time it takes to get additional signals to look at," he says. "It has the Novas Debussy waveform, so it starts to look just like a simulator. From the time we find a failure, bring up the waveforms, and have the designer sitting next to us fixing the problem, resynthesizing the emulator, and rerunning it, takes an hour or two in some cases." EDN

REFERENCE

1 Moretti, Gabe, "Hardware tools aid engineers in design verification," *EDN*, Aug 30, 2001, pg 77, www.edn.com/article/CA152890.html.

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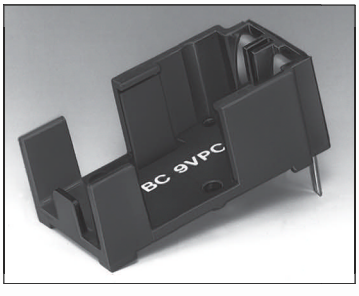
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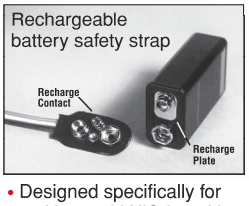


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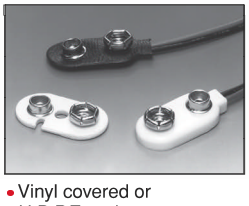


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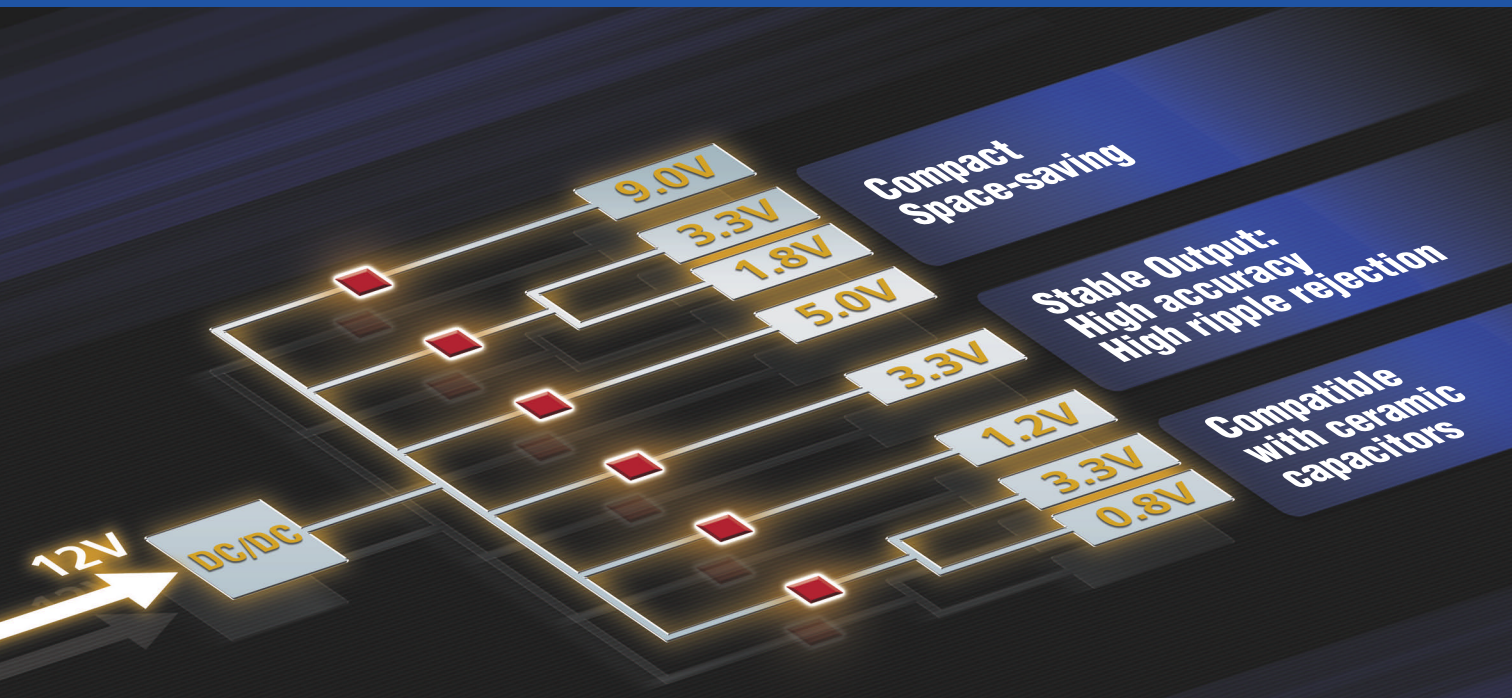


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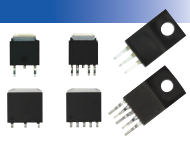
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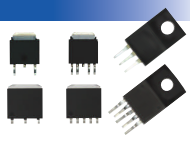
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BA□□BC0W	1.5, 1.8, 2.5, 3.0, 3.3, 5.0, 6.0, 7.0, 8.0, 9.0, 10.0	1.0	18
BA00BC0W	1.5 to 12 Variable	1.0	18

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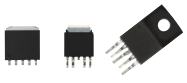
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BA00JC5W	1.5 to 12 Variable	1.5	18

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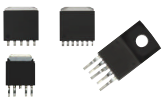
- Space is conserved due to ceramic capacitor compatibility (BA3258).
- Stable output with a high ripple rejection rate of 74dB (BA33D□□).



Part No.	Output Voltage (V)	Output Current (A)	Voltage Resistance (V)
BA3258	1.5, 3.3	1.0	18
BA33D□□	3.3/1.5, 3.3/1.8	0.5	18

Fixed / Variable Dual-output 18V Rated Voltage

- Independent two-system input type regulators contribute to greater power reduction.
- The variable output section can be easily and arbitrarily externally between 0.8V and 3.3V.



Part No.	Output Voltage (V)	Output Current (A)	Voltage Resistance (V)
BA3259	3.3, 0.8 to 3.3 Variable	1.0	18
BA30E00W	3.3, 0.8 to 3.3 Variable	0.6	18

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BY WARREN WEBB • TECHNICAL EDITOR

Mobile robots GET SERIOUS

AFTER YEARS OF SERVING HOBBYISTS AND MOVIE-MAKERS, A SERIES OF WORLD EVENTS MAY ELEVATE MOBILE ROBOTS TO TECHNOLOGY'S "NEXT BIG THING."

Although the concept and operational hardware for mobile robots have been around for decades, a rash of natural disasters and continuing military conflict have prompted designers to take a fresh look at the capabilities of this technology. The idea of an electromechanical device's replacing one or more humans in a hazardous or potentially dangerous situation has become the mantra of military, law-enforcement, aerospace, and exploration projects. Ranging from simple wheeled vehicles with a camera to unmanned aircraft with armaments, mobile-robotic technology has saved untold numbers of lives and become the favorite subject of new development projects. These applications have limited hardware resources and require real-time operation, compact mechanical design, battery operation, and economical software—requirements that embedded-system design shares. As such, robotic-control-system design is a logical next step for embedded-system-design teams.

Current products represent the leading edge of mobile-robotic design. For example, iRobot Corp's rugged, lightweight PackBot EOD (explosive-ordnance-disposal) robot conducts EOD, hazardous-material handling, search and surveillance, and hostage-rescue tasks for bomb squads, SWAT (special-weapons-and-tactical) teams, and military units (**Figure 1**). The PackBot's manipulator system can reach as far as 2m in any direction to disrupt improvised explosive devices, military ordnance, land mines, and other incendiary devices. One operator can carry and deploy the PackBot EOD, which weighs approximately 53 lbs. The chassis offers eight payload bays, each with interchangeable payload modules, such as video, audio, chemical, and biological sensors; mine detectors; ground-penetrating radar; and extra power. A ruggedized operator-control unit provides wireless-remote management and sensor display. Stressing the cost savings of robotics technology, Colin Angle, chief executive officer and co-founder of iRobot, says, "The US engagement in global conflicts has stressed our military and financial resources far beyond our original planning. More than half of our active-duty units are deployed abroad, and one in three reserve units were mobilized in the last four years. The bottom line is that expenditures are growing at an exponential rate, and a basic technological change is necessary to keep the cost and manpower requirements under control."

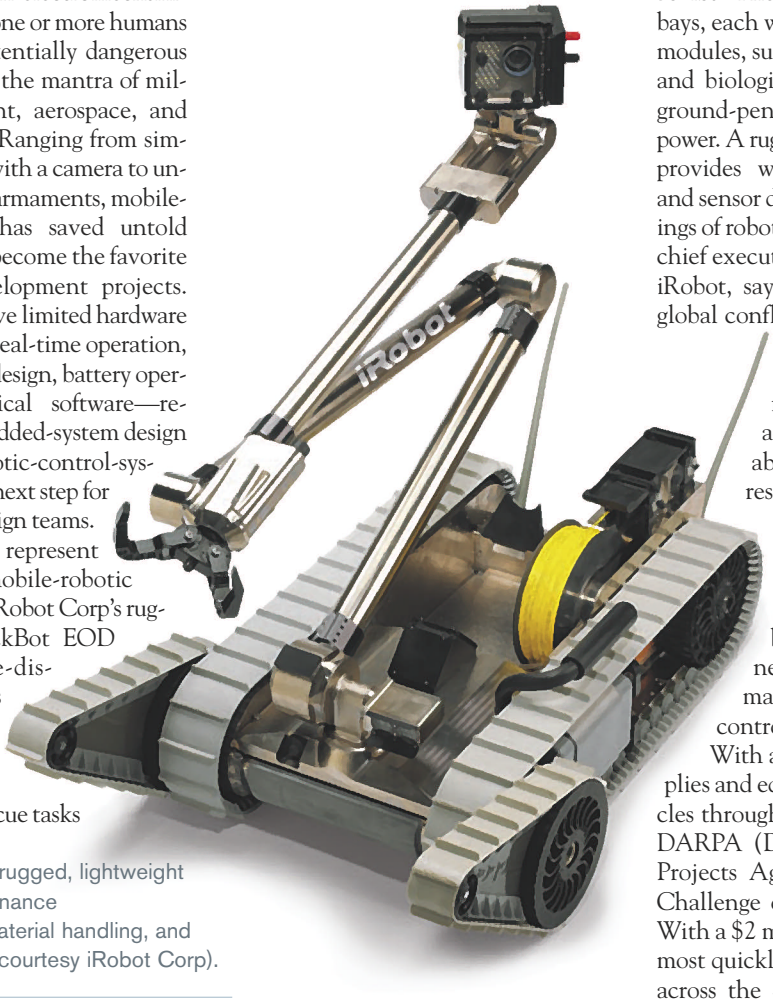


Figure 1 PackBot is a rugged, lightweight robot for explosive ordnance disposal, hazardous-material handling, and surveillance activities (courtesy iRobot Corp).

With an eye toward delivering supplies and equipment in unmanned vehicles through a hostile environment, the DARPA (Defense Advanced Research Projects Agency) sponsored its Grand Challenge on Oct 8, 2005 (**Figure 2**). With a $2 million prize for the team that most quickly finished a designated route across the Southwest's Mojave Desert,



AT A GLANCE

- Military, law-enforcement, and industrial organizations use unmanned mobile robots to reduce human exposure to hazardous environments.
- The embedded control systems for mobile robots range from autonomous to human-in-the-loop systems.
- Designers must choose from hundreds of variations of ac, dc, and stepper motors to satisfy each application's unique requirements.
- Off-the-shelf development kits simplify the integration of a motor's mechanical properties with an embedded-system application.

the contest was designed to accelerate research and development in autonomous ground-vehicle technology that will help save lives on the battlefield. DARPA Director Anthony J Tether notes, "This event is a challenge for US ingenuity. It brings together individuals and organizations from the research-and-development community, industry, government, the armed services, academia, and professional societies and from the ranks of students, backyard inventors, and automotive enthusiasts." Stanford University's team pocketed the cash with its "Stanley" robotic car, which the team based on a diesel Volkswagen Touareg R5, which covered the 132-mile course in just less than seven hours with an average speed of 19.1 mph. Stanley comes with seven Pentium M processors, a global-positioning system, a radar system, four laser-range finders, and a stereo-camera system. It also has an inertial-measurement unit that can estimate how the vehicle is tilted relative to the ground. Four other teams also completed the course.

ROBOT MOTION

Motion control is the foundation of robotics, and designers most often implement it by computer control of electric motors or actuators. Embedded-system designers have used electromagnetic-control circuits since the early days of electronics to energize motors, relays, solenoids, and speakers, but current motion-control techniques are more complex, because system requirements call for precision motion that is coordinated among multiple motors or actuators. Designers usually opt for dc or stepper motors for precision motion control. You can apply each motor type in open-loop situations or with feedback from the motor itself or other portions of your application to guarantee accuracy. Each of the motor types has myriad variations with corresponding advantages, drawbacks, and best-suited applications.

Stepper motors are among the most popular robotic-motion-control devices because they move in discrete steps, provide accurate angular-position information, and are relatively easy to control. The rotor of a stepper motor consists of permanent magnets arranged in a series of poles that determine the step size. The stator includes multiple windings to create a magnetic field that interacts with the rotor's permanent magnets. As a sequence of pulses from a control circuit turns the stator windings on and off, the motor rotates in the forward or reverse direction. Reversing the stator-pulse sequence changes the direction of rotation, and the frequency of the pulses controls the speed. To make a stepper motor rotate, you must constantly turn on and off the windings. Conversely, if you constantly energize one winding, the motor stops rotating and maintains an angular position with its specified holding torque.

Modern dc motors find wide use in robotic applications, which require precise control of rotational speed or torque. A dc motor rotates by the interaction of two magnetic fields. The stator creates a fixed magnetic field with a permanent magnet or energized electromagnet, and the rotating armature or rotor includes a series of electromagnets that generate a magnetic field when current flows through one of its windings. For a brushed-dc motor, a commutator on the rotor and brushes on the stator energize individual windings as the motor rotates. The opposite polarities of the energized rotor winding and the stator magnet attract, causing the rotor to move until it aligns with the stator field. Just as the rotor reaches alignment, the brushes move across the commutator and energize the next winding to maintain motion.

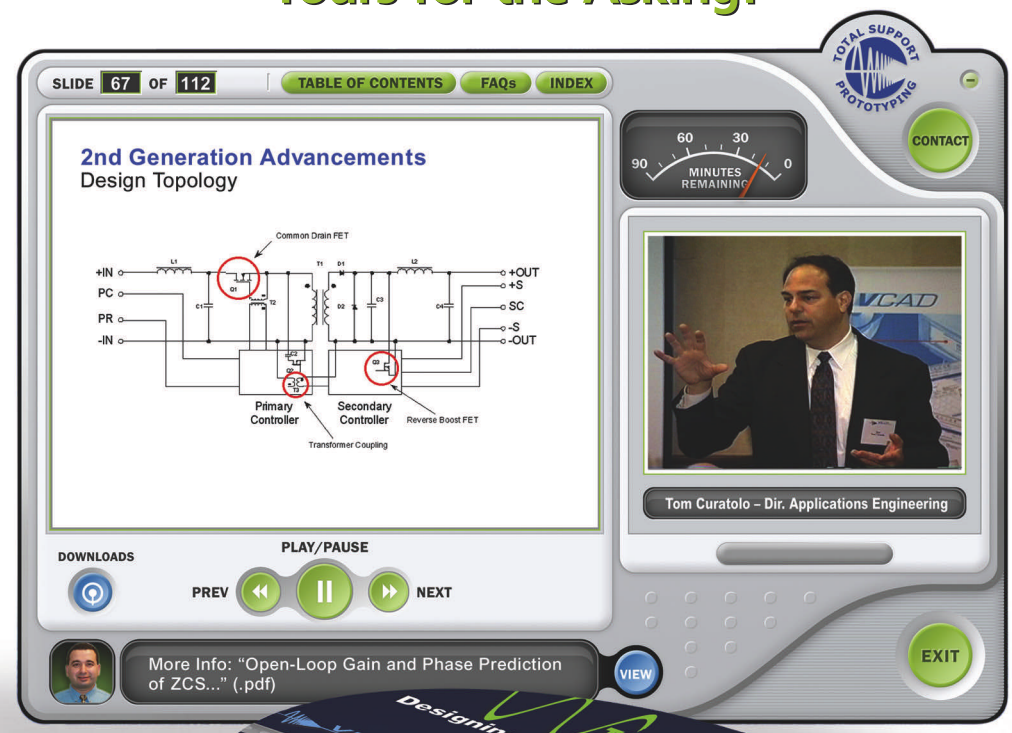
Speed in motors is proportional to the applied voltage, and output torque is proportional to the current. Robotic control of dc motors is a challenge, because you



Figure 2 The Defense Advanced Research Projects Agency recently awarded a $2 million prize for navigating a desert course in an unmanned robotic vehicle.

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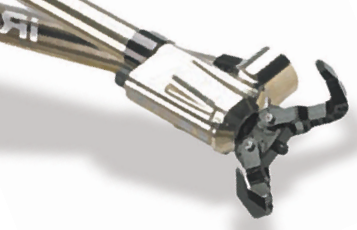


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must vary the speed of the dc-motor during operation. The most popular approach to efficient dc-motor operation is to apply a PWM (pulse-width-modulated) square wave with an on-to-off ratio corresponding to the desired speed. The motor acts as a lowpass filter to translate the PWM signal into an effective dc level. PWM-drive signals are popular because a microprocessor-based controller can easily generate them. Although a precise pulse width regulates the motor's speed, the actual PWM frequency is variable, and designers should optimize it to prevent motor chatter, audible noise, and RFI. To reverse a dc motor, you must reverse the direction of the current in the motor; most designers use four switching devices arranged in an H pattern for this purpose.

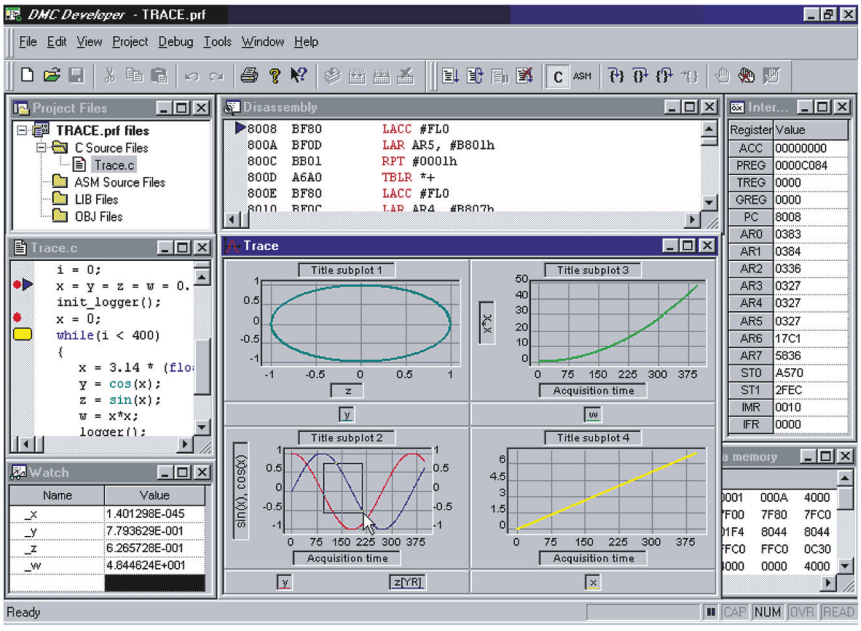


Figure 3 A dedicated processor in the MCK240 DSP motion-control kit from Technosoft calculates real-time motion-control trajectories.

BRUSHLESS HALL EFFECT

A popular variation of the dc motor eliminates the electrically noisy and maintenance-prone brushes but sacrifices controller simplicity. The brushless-dc motor is basically a synchronous motor with permanent magnets on the rotor and windings on the stator. Stator windings are arranged in a three-phase Y connection and produce trapezoidal torque characteristics. The energized stator windings create electromagnet poles that attract the rotor and generate torque. By using an appropriate sequence to apply voltages to the stator phases, you can create and maintain a rotating field on the stator. You must synchronize the stator current with the rotor field to generate a torque. Most brushless-dc motors use Hall-effect sensors to read the motor's rotor position and enable the controller to switch the three winding phases on and off in the proper sequence to produce rotary motion.

As the motion-control problem becomes more complex through coordinated moves or intricate motion profiles, designers have turned to dedicated processors or DSPs to calculate real-time trajectories. For example, the MCK240 DSP motion-control kit from Technosoft is an evaluation and development package for the Texas Instruments TMS320F240 DSP controller. The kit comes with an onboard 50W, three-phase inverter and a brushless motor with Hall sensors and a 500-line encoder. Built-in current feedback from the inverter low-side legs or dc path allows the development and implementation of a large set of control algorithms, including sensorless approaches. All communication between the PC and the DSP board occurs through the RS-232 interface using flash-resident monitoring software with downloading, uploading, debugging, and inspection capabilities. The kit includes a graphical motion-control, evaluation, and analysis software package, along with a set of ready-to-run examples (**Figure 3**). The MCK240 costs approximately $1250.

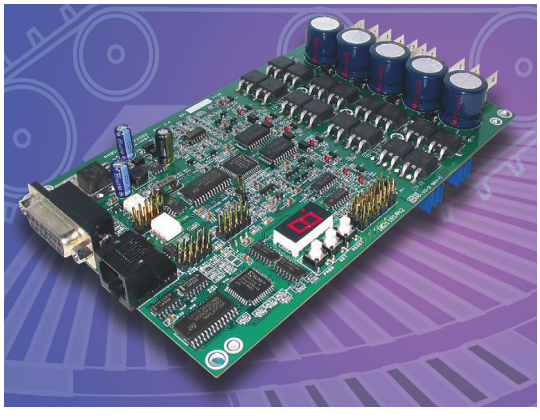


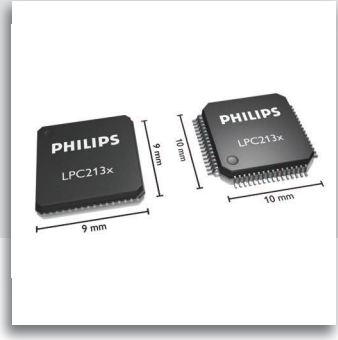
Figure 4 Roboteq's dual-channel dc-motor controller continuously drives as much as 60A on each channel at voltages as high as 40V.

Several motion-control vendors offer off-the-shelf controllers for mobile-robotics systems. Roboteq Inc offers a microcomputer-based, dual-channel dc-motor controller that can directly and continuously drive as much as 60A on each channel at voltages as high as 40V. The AX3500 targets designers of mobile-robotic vehicles, including automatic guided vehicles, underwater remotely operated vehicles, and mobile robots for exploration, hazardous-material-handling, military, and surveillance applications (**Figure 4**). The OEM version comes on a 4.2×6.75-in. board and accepts commands from a serial-port interface or a standard remote-controlled radio for robot applications. With the serial port, developers can use the AX3500 to design fully autonomous or semiautonomous robots by connecting it to single-board computers, wireless modems, or wireless-LAN adapters.

LPC2000 Family

Part Number	Memory		Timers/ PWM		Serial Interfaces				A/D (10b)	D/C (10b)	I/O	Inter-rupts	F max	Temp. Range	Package
	Flash	RAM	# of Timers	Ch.	UART	I²C	SPI	CAN	# of ch.	# of ch.	Pins	(Ext.)	(Mhz)		
LPC2104	128K	16K	4*	6	2	1	1	–	–	–	32	16(3)/16	60	0° to +70°	LQFP48
LPC2105	128k	32K	4*	6	2	1	1	–	–	–	32	16(3)/16	60	0° to +70°	LQFP48
LPC2106	128K	64K	4*	6	2	1	1	–	–	–	32	16(3)/16	60	0° to +70° -40° to +85°	LQFP48
LPC2114	128K	16K	4*	6	2	1	2	–	4/10	–	46	19(4)/16	60	-40° to +85°	LQFP64 HVQFN64
LPC2119	128K	16K	4*	6	2	1	2	2	4/10	–	46	19(4)/16	60	-40° to +85°	HVQFN64 LQFP64
LPC2124	256K	16K	4*	6	2	1	2	–	4/10	–	46	19(4)/16	60	-40° to +85°	HVQFN64 LQFP64
LPC2129	256K	16K	4*	6	2	1	2	2	4/10	–	46	19(4)/16	60	-40° to +85°	HVQFN64 LQFP64
LPC2131	32K	8K	4*	6	2	2	2	–	0	0	47	22(4)/16	60	-40° to +85°	LQFP64
LPC2132	64K	16K	4*	6	2	2	2	–	1	1	47	22(4)/16	60	-40° to +85°	HVQFN64 LQFP64
LPC2134	128K	16K	4*	6	2	2	2	–	2/8	1	47	22(4)/16	60	-40° to +85°	LQFP64
LPC2136	256K	32K	4*	6	2	2	2	–	2/8	1	47	22(4)/16	60	-40° to +85°	LQFP64
LPC2138	512K	32K	4*	6	2	2	2	–	2/8	1	47	22(4)/16	60	-40° to +85°	HVQFN64 LQFP64
LPC2194	256K	16K	4*	6	2	1	2	4	4/10	–	46	19(4)/16	60	-40° to +85° -40° to +125°	LQFP64
LPC2210	Ext.	16K	4*	6	2	1	2	–	8/10	–	76	19(4)/16	60	-40° to +85°	LQFP144
LPC2212	128K	16K	4*	6	2	1	2	–	8/10	–	112	19(4)/16	60	-40° to +85°	LQFP144
LPC2214	256K	16K	4*	6	2	1	2	–	8/10	–	112	19(4)/16	60	-40° to +85°	LQFP144
LPC2290	Ext.	16K	4*	6	2	1	2	2	8/10	–	76	19(4)/16	60	-40° to +85°	LQFP144
LPC2292	256K	16K	4*	6	2	1	2	2	8/10	–	112	19(4)/16	60	-40° to +85°	LQFP144
LPC2294	256K	16K	4*	6	2	1	2	4	8/10	–	112	19(4)/16	60	-40° to +85° -40° to +125°	LQFP144

*Includes Watchdog Timer and Real-Time Clock



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The controller's two channels can operate independently, or you can combine them to set the direction and rotation of a vehicle by coordinating the motion on each side of the vehicle. The motors operate in open- or closed-loop speed or position modes. The AX3500 includes inputs for two quadrature encoders and four limit switches for speed and odometer measurement. The AX3500 features intelligent current sensing and automatically limits each channel's power output to user-preset values as high as 60A. The AX3500 is available now at $395 (one) and comes with an interface cable and PC-based configuration software.

HOBBY CONTRIBUTIONS

Mobile robotics receives a huge amount of research, development, software, and trial-and-error testing from engineers and hobbyists having fun with combat robots. These fighting machines use dc motors, batteries, and remote-control electronics, along with an array of weapons in an attempt to subdue or disable an opponent. The agility of these robots directly depends on the dc-motor controller. Several companies provide off-the-shelf controllers to supply the high voltage and current that a battle situation requires. However, one of the most useful spin-offs for design engineers is the OSMC (Open Source Motor Controller) project. This project began as an Internet-hosted collaborative effort to design and implement a high-power, H-bridge motor-control system for permanent-magnet dc motors targeting battle robots. You can purchase kits or download free schematics, parts lists, and software for the OSMC boards from www.robot-power.com. You can also join the OSMC project and follow new developments at http://groups.yahoo.com/group/osmc/.

Mobile robotics is a new and growing industry with diverse military, law-enforcement, aerospace, medical, and home applications appearing weekly. For example, Daniel Zanini, senior vice president and program manager at research and engineering company SAIC, says, "Robotics will play a major role in our future combat systems. Unmanned aircraft, submarines, and land vehicles, along with conventional forces, will become nodes in a huge integrated network system, allowing commanders to determine the status and deploy resources from a computer screen." Targeting consumers, iRobot has shipped more than 1.2 million Roomba mobile robots for automated home vacuuming. A constant flow of new technology, such as improved motors, better control algorithms, and more efficient controllers, gives embedded-system designers plenty of tools and opportunities to participate in robotics development. Like it or not, mobile robots will continue to replace, augment, or support human activity in the future. Maybe some of those weird science-fiction stories were right on. EDN

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You can reach Technical Editor Warren Webb at 1-858-513-3713 and wwebb@edn.com.

I²C Data Converters

High Performance Analog Solutions from Linear Technology

Data converters, both analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), are increasingly in demand for applications that digitally monitor and control system performance. Precision requirements are continuously increasing in these applications, as well as the number of converters per system. However, the available board space is decreasing rapidly. High performance devices with serial interfaces, the I²C bus in particular, help to support most of these conflicting demands.

Linear Technology has introduced 16-bit ADCs and DACs featuring the I²C interface and tiny packages. The LTC®2480 family of No Latency Delta-Sigma™ ADCs includes both 16-bit and 24-bit devices in the tiny 3mm x 3mm DFN package. The LTC2600 family of low power, voltage output 16-bit DACs start in the 3mm x 3mm DFN package for a single DAC and range up to an octal DAC in a 16-pin SSOP.

I²C Basics

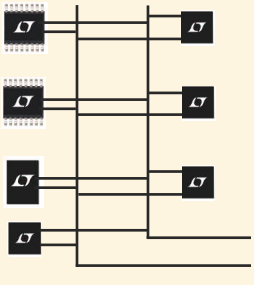
The I²C protocol uses a 2-wire open-drain interface, supporting multiple devices and masters on a single bus. The connected devices only pull the bus wires LOW and never drive the bus HIGH. The bus wires are externally connected to a positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. Data on the I²C bus transfers at rates of up to 100kbit/s in the Standard-mode and up to 400kbit/s in the Fast-mode.

Each device on the I²C bus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave.

Smallest 16-bit I²C V_{OUT} DAC Family

The LTC2605, octal 16-bit voltage output DAC with an I²C serial interface in a 16-pin SSOP package, achieves the industry's smallest footprint for octal DACs while improving DC performance over competitive products. The device's guaranteed mono-

Table 1. High Resolution DACs and ADCs with I²C and Tiny Packages

LTC2605	Octal, 16-bit DAC		24-bit, Delta-Sigma ADC with Internal Temp. Sensor	LTC2485
LTC2609	Quad, 16-bit DAC		16-bit, Delta Sigma ADC with Internal Temp. Sensor and Programmable Gain	LTC2481
LTC2607	Dual, 16-bit DAC		16-bit, Delta Sigma ADC	LTC2483
LTC2606	Single, 16-bit DAC			

I²C Data Converters

tonic performance, small size and low power make it ideal for digital calibration, trim/adjust and level setting applications in a wide variety of products.

The LTC2605's output buffers deliver excellent drive capability over

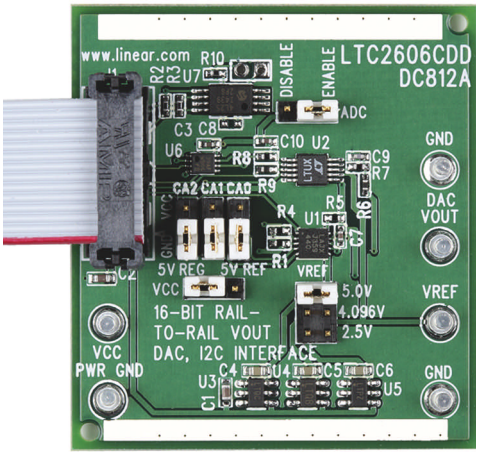


Figure 1. LTC2606 16-Bit V_{OUT} DAC (U1) Requires Just 3mm x 3mm Board Space

their entire 2.7V to 5.5V supply voltage range. The DAC outputs directly drive capacitive loads up to 1000pF or current loads up to 15mA and maintain good linearity to within millivolts of V_{CC} or ground. The low output offset (9mV max) provides a starting code voltage closer to ground than competing devices. In addition, low output voltage noise ($15\mu V_{P-P}$) reduces the need for output filtering. A full-scale transition on seven of the eight DACs causes less than 10µV change in the eighth DAC, effectively eliminating crosstalk as a source of error. The LTC2605's low 250µA supply current per DAC at 3V and 1µA maximum shutdown current are ideal for battery-powered applications.

The 2-wire I²C compatible interface allows independent control of each DAC by means of a flexible input control word. The LTC2605 provides 27 user-selectable slave addresses, allowing several LTC2605s on the same bus and minimizing address conflicts with other components.

The LTC2605 is one device in a family of compact DACs from octals to singles with either I²C or SPI interfaces (Table 2). The LTC2615/LTC2615-1 and LTC2625/LTC2625-1 are pin-compatible 14-bit and 12-bit octal DACs, offering multiple price/performance options for one design. The "-1" versions power-on and reset to mid-scale, whereas the other versions power-on and reset to zero scale. Quad versions (LTC2609) in the same size package feature separate reference inputs for each DAC and a common zero scale input that allows for offset adjustment. Duals (LTC2607) in the 3mm x 4mm DFN package are also available to complement the smallest member of the family, the single LTC2606 in the 3mm x 3mm x 3mm DFN package, see figure 1.

16- to 24-Bit Delta Sigma ADC Family with Easy Drive Input Current Cancellation Simplifies Front-End Signal Conditioning

The LTC2481 is part of a series of delta-sigma ADCs featuring a novel front-end design that can directly digitize a wide range of sensors. The Easy Drive™ technology results in zero average differential input current, simplifying the design of front-end signal conditioning circuits and allowing the ADC to be driven directly from bridges, RTDs, thermocouples and other high impedance sensors. The LTC2481 is the first device to directly and accurately measure high impedance input sources without the use of an internal buffer, eliminating the drawbacks of on-chip buffering. The device eases design by incorporating an internal oscillator, transparent auto calibration and a wide input range that extends beyond the supply rails, and eliminating the need for initialization and calibration registers and invalid data associated with digital filter settling delays.

Table 2. I²C V_{OUT} DAC Family

Resolution	Single	Dual	Quad	Octal
16-bit	LTC2606	LTC2607	LTC2609	LTC2605
14-bit	LTC2616	LTC2617	LTC2619	LTC2615
12-bit	LTC2626	LTC2627	LTC2629	LTC2625

The input stage of traditional delta-sigma ADCs uses a switched capacitor network that rapidly switches between input, reference and ground at rates up to 10MHz as a function of the input signal level. Each time these capacitors are switched to the ADC input, significant charge/discharge current pulses are generated, making it difficult for the preceding op amp to drive. It also severely limits the time constant of input RC networks favored by designers for additional signal filtering. With the LTC2481 series, charge/discharge current pulses are balanced. When summed over the entire conversion cycle, the total differential input current is zero, independent of the differential input voltage, common mode input voltage, reference voltage, or output code. For the first time, external RC networks with large time constants may be placed directly in front of high resolution delta-sigma ADCs without degrading their DC accuracy.

The LTC2481 provides 16-bit resolution and features exceptional accuracy with 2ppm INL, 1ppm offset and 15ppm full-scale errors. The device can be configured through an I^2C interface to provide a programmable gain from 1 to 256 in 8 steps, to digitize an external signal or internal temperature sensor, reject line frequencies (50Hz, 60Hz or simultaneous 50Hz/60Hz) as well as a 2x speed-up mode (15Hz). The LTC2481 has two address pins, enabling one of six possible addresses. The internal temperature sensor is proportional to absolute temperature (PTAT) and accurate to the same level as the external signal, making the device suitable for temperature compensation of low level sensors. Linear Technology also offers a version without the internal temperature sensor or programmable gain (LTC2483) as well as a 24-bit version with the temperature sensor, but without programmable gain (LTC2485). The entire family features no latency conversions for simple multiplexing, highly accurate internal oscillators with guaranteed line frequency rejection, precise DC specifications and the ease-of-use common to all of Linear Technology's LTC2400 ADC converters. All three parts are pin-compatible in the 3mm x 3mm 10-pin DFN package and there are similar versions available with the SPI serial interface.

Wide Range of I^2C Devices

The I^2C bus is popular for a range of control and monitoring functions in addition to data conversion. Table 3 shows the range of devices offered by Linear Technology supporting the I^2C or SMBus interface protocols. As the number of nodes increases and the bus is distributed over connectors and backplanes, the total capacitance increases and signal integrity problems may occur. A bus buffer effectively isolates the capacitance, solves some signal integrity problems and allows the bus to be used in high availability systems where live insertion and removal of circuit boards is required. These buffers are unique functions in addition to products such as battery chargers, system controllers, DC/DC converters and data converters with an I^2C interface.

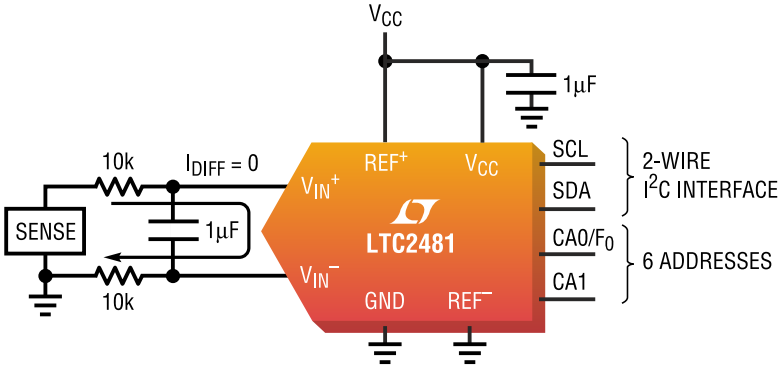


Figure 2. LTC2481 Allows Measurement of High Impedance Sources

I²C Data Converters

Table 3. Range of Products from Linear Technology Supporting I²C

	Function	Features	Part Number
BUS BUFFERS	I²C Accelerator	Improves I²C or SMBus Rise Time Transition	LTC1694
	Bus Buffer	Isolates Input and Output Capacitance	LTC4300
	Bus Buffer with Level Translation	Translates 1V Signals to 3.3V or 5V Logic	LTC4301
	Smart Bus Buffer	Connect Bus Segments with I²C Commands	LTC4302
	Bus Buffers with Stuck Bus Recovery	Automatic Disconnect of SDA/SCL Lines when Bus is Stuck Low	LTC4303/4304
	2:1 Bus Multiplexer with Buffer	1:2 2-Wire Multiplexer/Switch and Bidirectional Buffer	LTC4305
	4:1 Bus Multiplexer with Buffer	1:4 2-Wire Multiplexer/Switch and Bidirectional Buffer	LTC4306
SYSTEM CONTROLLERS	Fan Speed Controller	0.75Ohm 180mA Linear Regulator	LTC1695
	Dual Fan Speed Controller	Two 8-Bit Current DACs	LTC1840
	3.2Gbps VCSEL Driver	Digital Setup and Control with I²C I/O	LTC5100
	1kHz - 68MHz Serial Port Programmable Oscillator	Frequency Error <1.1% Over All Settings	LTC6904
DATA CONVERTERS	Single-Ended 8-Ch./ Differential 4-Ch. Analog Multiplexer	Single 2.7V to ±5V Supply Operation	LTC1380/1393
	10-Bit Current Output DAC	Precision 50µA, ±1.5% Full-Scale Output Current	LTC1427
	10-Bit Voltage Output DAC	SOT-23 Package, Ultralow Power	LTC1663/1669
	16-Bit Delta-Sigma ADC	Internal Temperature Sensor, Programmable Gain	LTC2481
	16-Bit Delta-Sigma ADC	Low Noise, Tiny Package, Low Cost	LTC2483
	24-Bit Delta-Sigma ADC	Internal Temperature Sensor	LTC2485
	16-/14-/12-Bit Octal Voltage Output DACs	Low Power, Low Offset, Tiny Package	LTC2605/15/25
	16-/14-/12-Bit Single Voltage Output DACs	Low Power, Low Offset, Tiny Package	LTC2606/16/26
	16-/14-/12-Bit Dual Voltage Output DACs	Low Power, Low Offset, Tiny Package	LTC2607/17/27
	16-/14-/12-Bit Quad Voltage Output DACs	Low Power, Low Offset, Tiny Package	LTC2609/19/29
HOT SWAP CONTROLLERS	Quad -48V Power over Ethernet (PoE) Controllers	IEEE 802®.3af Compliant PD Detection and Classification	LTC4258/4259A
	CompactPCI Hot Swap Controller	Controls 3.3V, 5V, 12V and –12V Supplies	LTC4240
	+48V Hot Swap Controller	Internal 8-bit ADC	LTC4260
	-48V Hot Swap Controller	Internal 10-bit ADC	LTC4261
POWER MANAGEMENT	Programmable CCFL Switching Regulator	Grounded Lamp or Floating Lamp Configurations	LT1786F
	Dual High-SideSwitch Controller	Built-In Charge Pumps Drive N-Channel Switches	LTC1623
	SMBus VID Voltage Programmers	Compliant with Intel 5-Bit Mobile and Desktop VRM8.4 and VRM9.0 VID Specifications	LTC1699
	Dual High-Side Switch	Two 0.4Ohms/300mA N-Channel Switches	LTC1710
	No R_{SENSE}™ Step-Down DC/DC Controller	2% to 90% Duty Cycle at 200kHz	LTC1909
	Multidisplay LED Controller	Step-Up/Direct-Connect Fractional Charge Pump	LTC3206
	High Current Multidisplay LED Controller	17 Current Sources Available as MAIN, SUB, RGB, CAM and AUX LED Drivers	LTC3208
	Buck Regulator with Two LDOs	Intel xScale™ Microprocessor Power Manager	LTC3445
	Buck Regulator	Programmable Output for Intel xScale Processor	LTC3447
BATTERY CHARGERS	Dual Smart Battery System Manager	Allows Both Batteries to Discharge Simultaneously into Single Load with Low Loss (Ideal Diode)	LTC1760
	Smart Battery Charger Controller	±0.8% Voltage Accuracy; ±4% Current Accuracy	LTC4100

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BY JOSHUA ISRAELSOHN • CONTRIBUTING TECHNICAL EDITOR

A MATTER OF BALANCE: line-receiver CMR in real-world environments

FEW APPLICATIONS ALLOW YOU TO CONTROL THE SOURCE IMPEDANCE OF YOUR INCOMING SIGNALS, YET YOUR LINE RECEIVER'S CMR CAN HANG IN THE BALANCE.

Common interconnect methods satisfy bandwidth, impedance, noise-immunity, attenuation, and signal-run-length requirements for a broad range of applications with surprisingly few topologies. Among the more robust is the balanced line, which finds use in such disparate applications as industrial process control, medical sensing, professional audio, and high-speed digital communications, among others. The balanced line is particularly useful for long feeds in applications that require a high degree of noise immunity.

IN A PERFECT WORLD ...

Though balanced signal-processing structures do exist, most moderate-bandwidth applications do well implementing functions with single-ended structures and reserve balanced signal paths for longer interconnects. In such cases, interface circuits must convert single-ended signals to balanced differential outputs and provide sufficient signal current to drive the load impedance. On the other end of the rope, a line receiver must capture the differential signal and reject the common-mode component while converting the balanced signal back to single-ended (**Figure 1**).

Transformers offer a simple means of conversion between balanced and single-ended signal feeds and additionally provide galvanic isolation between the signal source and its load that can easily extend to several hundred volts and, with care, to beyond 1 kV. Most installations, however, demand a common-mode range of only a few volts, and the additional cost, weight, and size of the transformers are often undesirable.

An electronic alternative uses line-driver and line-receiver ICs to replace either or both transformers. The drivers simply provide a pair of antiphase outputs, often with local sense feedback (**Figure 2**). On the receiver side, however, replicating the transformer's high degree of symmetry is a challenge. Historically, the most successful circuit approaches have used a difference amplifier and exploited analog-IC manufacturers' ability to fabricate and precisely trim matching resistors (**Figure 3**).

By superposition, the difference amplifier's output is the sum of two terms: $V_O=V_{OA}+V_{OB}$. Kirchoff's Cur-

AT A GLANCE

- Electrically balanced signal feeds are subject to a variety of imbalancing influences that result in asymmetrical source impedances.
- Traditional balanced line receivers use difference amplifiers to recover the differential-mode and suppress the common-mode signal components.
- Source-impedance asymmetries reduce CMR (common-mode-response) performance in difference amplifiers and allow common-to-differential-mode conversion.
- An input bootstrapping method improves a receiver's CMR performance in the presence of a source-impedance asymmetry.

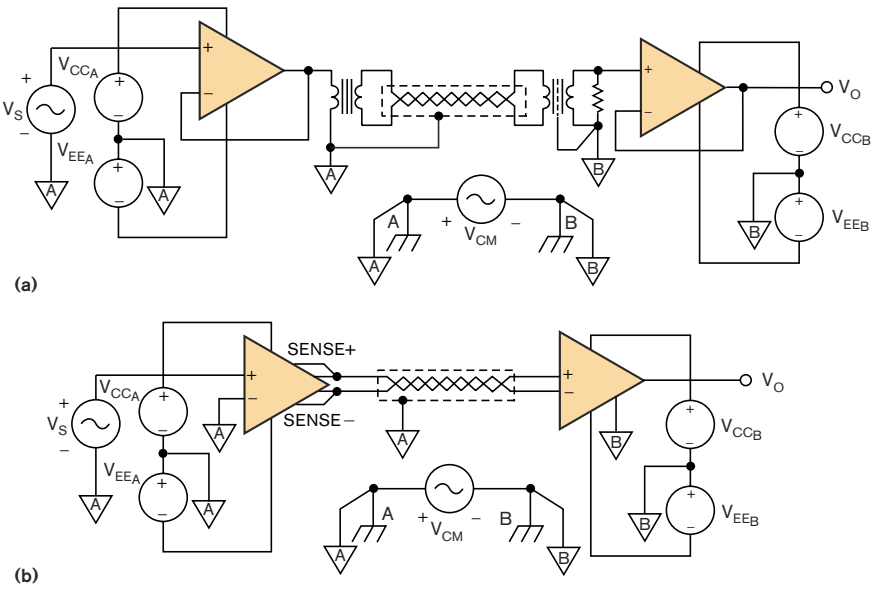


Figure 1 It's hard to beat transformer-coupled balanced feeds (a) for CMR performance and standoff voltage, but electrically balanced drivers and IC-balanced receivers (b) provide often-compelling economies.

rent Law applied to the inverting input requires that

$$\frac{V_{OA}}{R_2}+\frac{V_{CM}-\frac{V_D}{2}}{R_{SA}+R_1}=0,$$

from which one of the output terms directly derives:

$$V_{OA}=\left(\frac{V_D}{2}-V_{CM}\right)\left(\frac{R_2}{R_{SA}+R_1}\right).$$

The solution for the second term assumes that the amplifier is operating in its linear range, which forces the two inputs to equal potentials.

$$V_{OB}\left(\frac{R_{SA}+R_1}{R_{SA}+R_1+R_2}\right)=\left(V_{CM}+\frac{V_D}{2}\right)\left(\frac{R_4}{R_{SB}+R_3+R_4}\right).$$

Isolating the output term yields

$$V_{OB}=\left(V_{CM}+\frac{V_D}{2}\right)\left(\frac{R_{SA}+R_1+R_2}{R_{SB}+R_3+R_4}\right)\left(\frac{R_4}{R_{SA}+R_1}\right)$$

and a good reason to say nice things about whomever first pointed out the value of symmetrical structures:

If you let $R_{SB}=R_{SA}$, $R_3=R_1$, and $R_4=R_2$, the last expression collapses into

$$V_{OB}=\left(V_{CM}+\frac{V_D}{2}\right)\left(\frac{R_2}{R_{SA}+R_1}\right).$$

Adding the two terms confirms that, if properly balanced, this topology responds only to the differential-mode input and rejects the common-mode term.

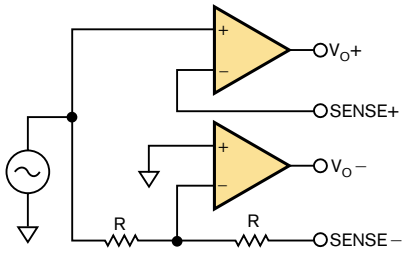


Figure 2 A simplified schematic of a unity-gain, electrically balanced driver includes local sense feedback, which can compensate for protection circuits.

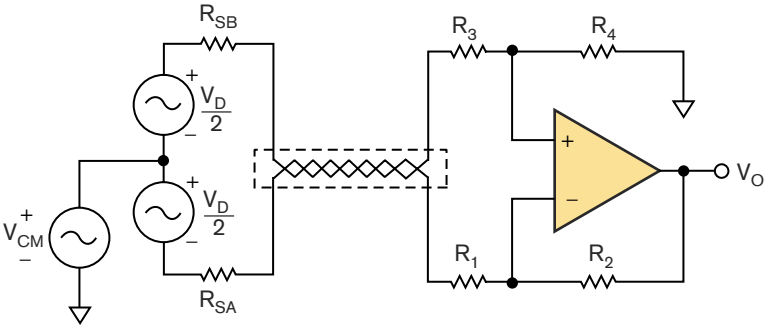


Figure 3 A balanced receiver, based on a difference-amplifier topology, rejects common-mode signals but passes differential-mode inputs. The CMR, however, depends on precisely trimmed resistors, R_1 to R_4, and a symmetrical source impedance.

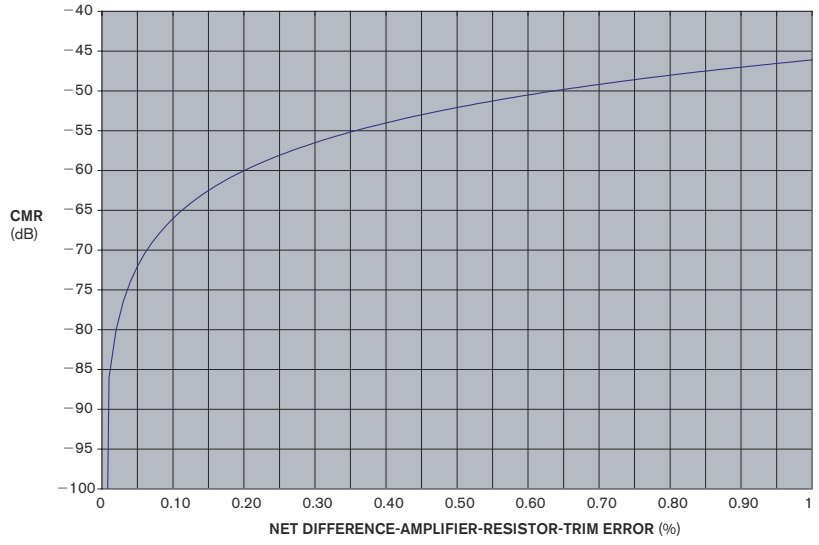


Figure 4 The balanced receiver's CMR performance degrades with resistor mismatches in the difference amplifier.

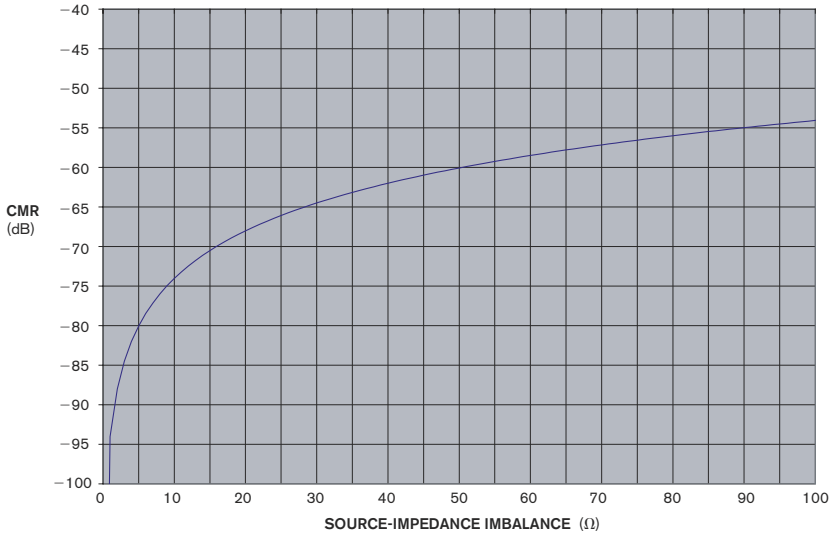


Figure 5 Asymmetries in the source impedance are indistinguishable from difference-amplifier-resistor mistrims. This curve models the CMR of a difference amplifier constructed with perfectly trimmed, 25-kΩ resistors and a signal source with 100Ω output impedance in each leg. An additional resistance in one leg rapidly degrades the CMR performance.

$$V_O = V_{OA} + V_{OB}$$
$$= \left(V_{CM} + \frac{V_D}{2} - V_{CM} + \frac{V_D}{2}\right)\left(\frac{R_2}{R_{SA} + R_1}\right)$$
$$= V_D\left(\frac{R_2}{R_{SA} + R_1}\right).$$

In practice, balanced-line-receiver manufacturers trim the on-chip resistors sufficiently well that the resultant ICs commonly provide minimum CMR (common-mode-response) specifications on the order of −70 dB or better at low frequencies (**Figure 4**, **references 1** and **2**). The sensitivity to the trim accuracy explains why, even with careful component matching, discrete balanced receivers tend toward comparatively marginal CMR performance.

IN THE REAL WORLD ...

Compared with typical source impedances, the difference amplifier's input resistors are reasonably large. Values in the few tens of kilohms are common, whereas source resistances usually fall in the area of a couple of hundred ohms. The source terms add to the difference amplifier's input resistances; the amplifier cannot distinguish between them. So, to the differential signal, the source impedance represents a minuscule gain error typically much smaller than 0.1 dB. To the common-mode signal, the source impedance has no effect as long as it is balanced across the two source legs. A source-impedance imbalance, however, is indistinguishable from a mistrim of the input resistors, the effect of which is readily calculable (**Figure 5**).

Impedance imbalances can arise in a variety of ways. Small asymmetries, on the order of a few ohms, can derive from component tolerances in the signal source's output-protection circuits. Connector-contact resistance can contribute several ohms more, particularly in temporary installations typical in sound-reinforcement systems for concerts, dramatic performances, lectures, meetings, and conferences; sound-capture facilities for on-location film, television, and sound recording; and signal-routing facilities in production studios and postproduction suites. Even with well-maintained, permanently installed equipment, a net imbalance of 5 or 10Ω is not out of the question—a condition that can degrade the CMR of an ideal receiver to −80 and −74 dB, respectively.

Connecting a piece of equipment with unbalanced outputs to a balanced input creates a source-impedance imbalance equal to the source's output impedance—often in the neighborhood of 100Ω. In this case, the CMR of an otherwise-perfect receiver degrades to −54 dB. Combining the two error sources—finite-trim accuracies and nonzero source imbal-

ances—results in the CMR performance typical of many balanced-signal feeds (**Figure 6**).

These values hold for low-frequency common-mode signals. Performance degrades further at higher frequencies with decreasing loop gain and the increasing influence of reactive imbalances within the interface circuit. This oft-ignored behavior should be of concern with the growing prevalence of switch-mode power supplies and construction techniques that pose challenges to ground-management designs—conditions that can invite broad-spectrum common-mode signals.

The most obvious method of desensitizing the receiver to a source-impedance asymmetry is to increase the difference amplifier's resistor values. This approach increases common-mode input impedance, which makes the source error proportionately smaller. Unfortunately, this approach simultaneously increases the differential-mode input impedance, which increases noise and dc offsets due to the amplifier's bias offset current (**references 3** and **4**).

WHITLOCK'S BOOTSTRAPS

The CMR of balanced receivers in the presence of source-impedance asymmetries has long been a simple fact of the interface topology. The traditional cost of resolving the issue has been that of a transformer-coupled interface. Ironically, perhaps, it was an expert in transformer design, Jensen Transformer President Bill Whitlock, who suggested a plausible solution for IC receivers (**references 5** and **6**). Whitlock's method buffers the incoming balanced signal, derives the common-mode level, and uses that signal to bootstrap the input resistors. The bootstrap path is ac-coupled, so the amplifier's input bias currents have a low-impedance return path. But the arrangement tracks the ac component of the common-mode signal, forcing the same ac potential to appear on both ends of the input resistors. The result is a substantial increase in the apparent common-mode input impedance and a reduced sensitivity to source-impedance asymmetries.

That Corp recently announced a family of IC receivers that implement Whitlock's bootstrap. The product announcement promised unusually high CMR even in the presence of asymmetrical source impedances. To compare the devices with other receivers, I checked the data sheets from the two leading suppliers of IC-balanced receivers, Analog Devices and Texas Instruments. Unfortunately, these data sheets don't characterize CMR performance with asymmetrical sources. They also do not reveal the input-circuit topology in any detail beyond the simplified schematics that accompany most ICs, so you cannot guess if they address the issue in some other way. The unanswered question then is: How much bet-

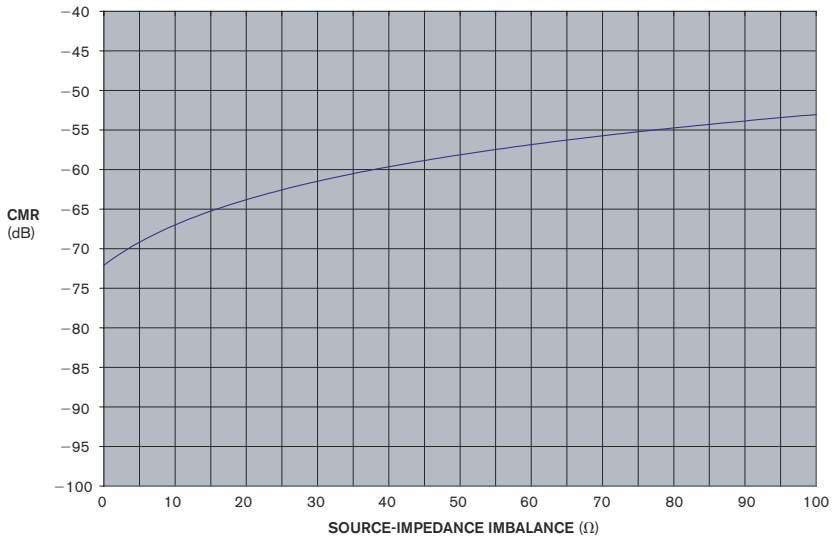
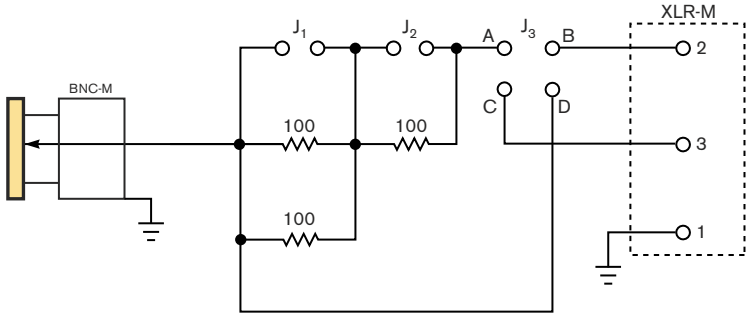


Figure 6 In practice, a combination of the residual error in the resistor trims and the source-impedance asymmetry limits an IC-balanced receiver's CMR performance. Here, the effect of a 0.05% error in R_1 (25 kΩ nominal) combines with a variable imbalance added to a source with 100Ω in each leg.



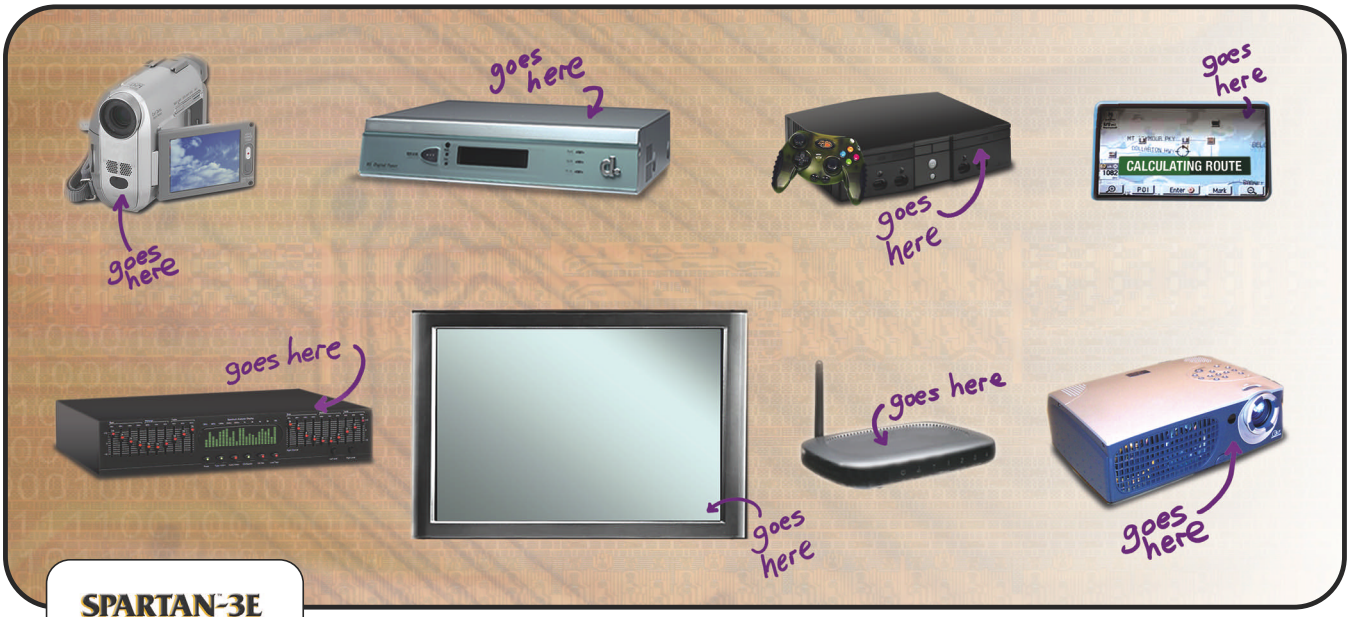
J_1	J_2	IMBALANCE (Ω)
SHORTED	SHORTED	0
OPEN	SHORTED	50
SHORTED	OPEN	100
OPEN	OPEN	150

J_3 A-C	J_3 B-D	IMBALANCE ON LOW PIN
J_3 A-B	J_3 C-D	IMBALANCE ON HIGH PIN

Figure 7 A simple fixture derives a common-mode test signal from the Audio Precision SYS-2722's analog generator. Jumpers J_1 and J_2 provide the means of injecting a source-impedance asymmetry of 0, 50, 100, or 150Ω. Jumper J_3 selects the output leg to which the fixture adds the asymmetry.

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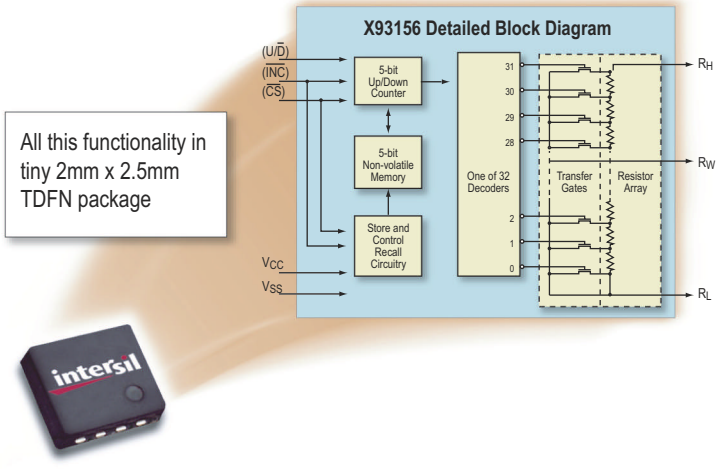
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- Available in 8-lead MSOP and TDFN packages
- Pb-free and RoHS compliant packaging available

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Description	Conditions	MIN	TYP	MAX	Unit
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	X93155	4.5	5	5.5	V
	X93156	2.7	-	5.5	V
End-to-end Resistence		35	50	65	kΩ
R_H, R_L Terminal Voltages		0	-	V_{CC}	V
Power Rating	R_{TOTAL} = 50 KΩ	-	-	1	Mw
Noise	Ref: 1kHz	-	-120	-	dBV
Wiper Resistance	X93156	-	-	1100	Ω
Wiper Current		-	-	0.6	mA
Resolution		-	3	-	%
Temperature (Industrial)		-40°C	-	+85°C	C

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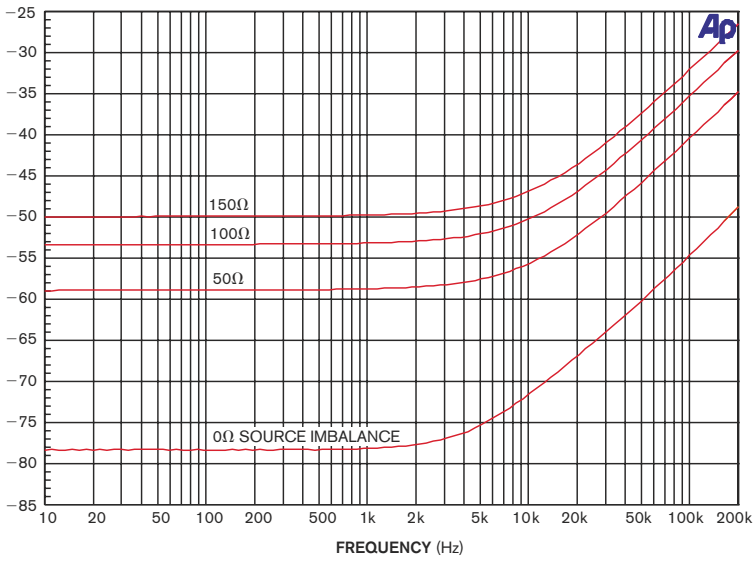


Figure 8 The Analog Devices SSM-2141's CMR performance agrees with a theoretical difference amplifier with matching error within about 0.02%.

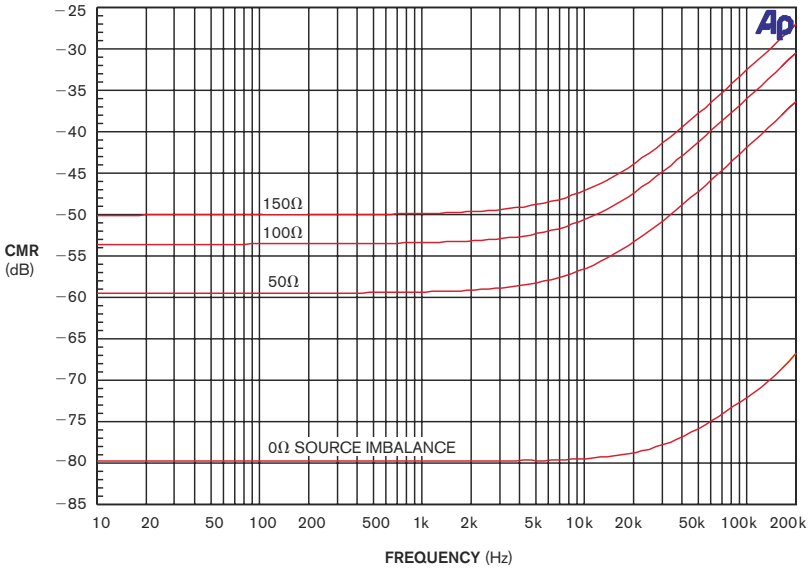


Figure 9 Like the SSM-2141, the Texas Instruments INA-134's CMR performance agrees with a theoretical difference amplifier with matching error within about 0.02%.

ter—if at all—could the CMR of the bootstrapped receiver be than those of the long-standing industry leaders?

TO THE BENCH!

A trivially simple fixture provides a CMR test signal from the Audio Precision SYS-2722 that serves as the core of *EDN*'s BenchPress test facility (**Figure 7**). Jumpers set the CMR source-impedance asymmetry to 0, 50, 100, or 150Ω. The three manufacturers provided samples of unity-gain balanced receivers—the Analog Devices SSM-2141, the

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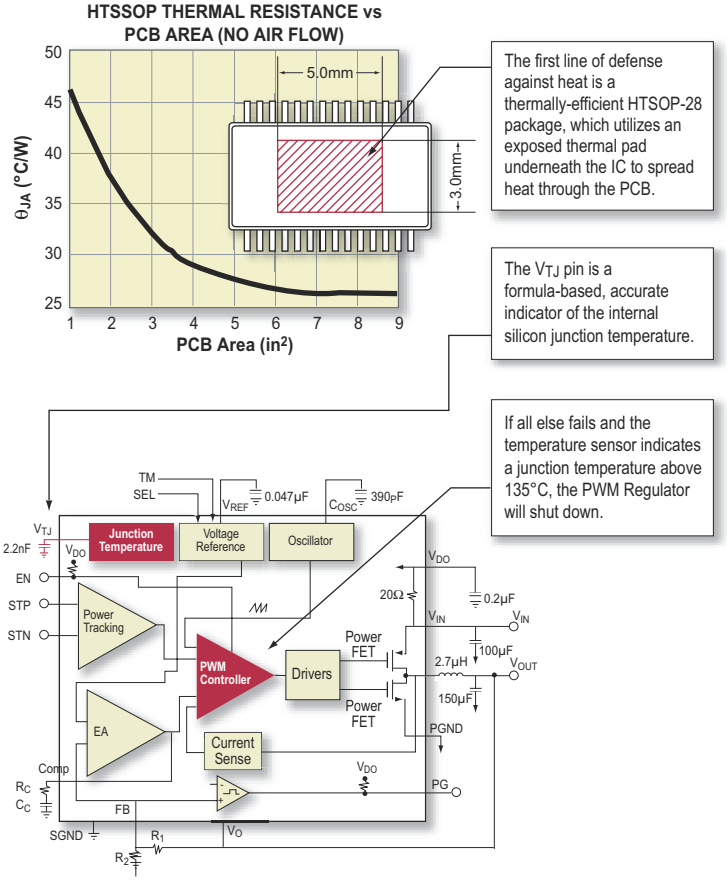
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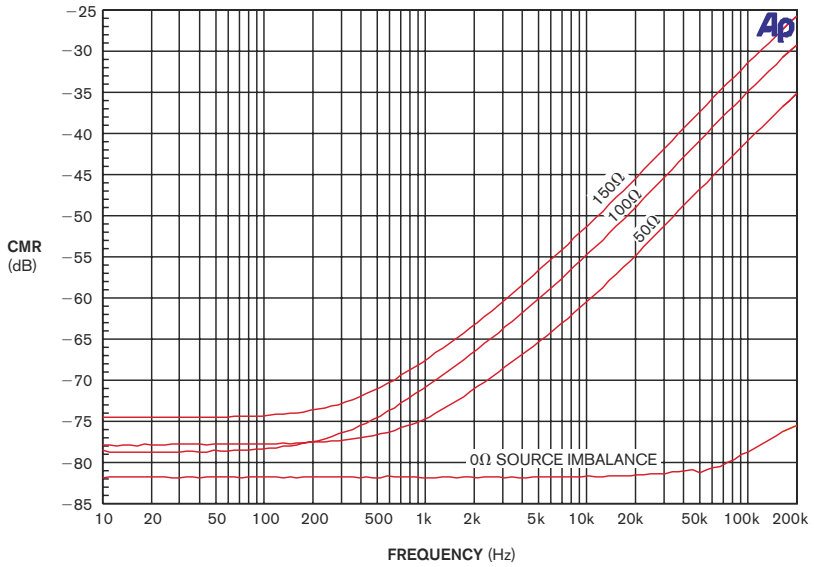


Figure 10 That Corp's That-1200, which implements Bill Whitlock's bootstrapped input structure, improves the balanced receiver's CMR performance in the presence of source-impedance asymmetries. The benefit begins to taper off at about the third harmonic of the power-line frequency.

Texas Instruments INA-134, and That Corp's That-1200. The SSM-2141 and the INA-134 share identical pinouts; the That-1200 differs in that a coupling capacitor for the bootstrap circuit uses the traditional pinout's unused and output-sense pins.

As is apparent from the CMR curves, the SSM-2141 (**Figure 8**) and INA-134 (**Figure 9**) provide similar common-mode performance. Low-frequency CMR with no source imbalance is on the order of −80 dB at low frequency, suggesting net resistor-matching errors on the order of 0.02%. Try doing that with a handful of discretes! A 50Ω source imbalance knocks about 20 dB off that figure, and another 10 dB comes off as the imbalance increases to 150Ω. Indeed, the CMR curves for the two devices are nearly congruent except in the fully balanced case in which the SSM-2141's CMR starts to decay at about 1 kHz, whereas the INA-134 holds on up to about 10 kHz. With 50- or 60-Hz power lines as the dominant common-mode concern, both devices turn in good performance with balanced sources and follow the theoretical curve for well-matched difference amplifiers driven by imbalanced source impedance (**figures 5** and **6**).

The That-1200 sample apparently has *incrementally* better resistor-matching errors than the SSM-2141 or INA-134 samples, which translates into a small improvement in CMR performance at low frequency with a well-balanced source (**Figure 10**). Based on the low-frequency CMR results, it appears that the samples *EDN* tested had net residual trim errors of about 0.015%. This figure does not give the 1200 a significant competitive claim over the traditional designs. It does show,

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however, in striking contrast to the other two receivers, the 1200's CMR performance with an asymmetrical source impedance: an 18-dB improvement at low frequency with a 50Ω imbalance, extending to a 25-dB improvement at 150Ω.

The bootstrap seems to work very well through the third harmonic of the line frequency. Beyond that point, the benefits start to degrade. The bootstrapped topology appears to provide at least incremental benefit throughout the audio spectrum, however. The CMR degrades, as you would expect, at a rate of 20 dB per decade at high frequencies (**figures 8** through **10**). Take care to minimize the high-frequency common-mode components deriving from switching supplies, EMI, or other sources: Slight asymmetries can convert these common-mode signal components to differential mode. Should that happen, only the antialiasing filter ahead of a digitizer prevents them from aliasing back into the audio band. EDN

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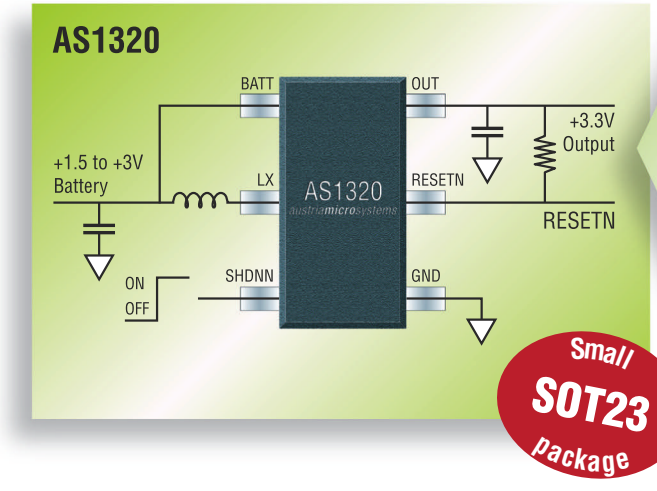
AUTHOR'S BIOGRAPHY

Contributing Technical Editor Joshua Israelsohn writes on analog and power technologies and applications. He is a graduate of the Massachusetts Institute of Technology, has 15 years' experience in electronic design, and has more than 25 years' experience in professional audio. He currently serves as director of technical information for International Rectifier. You can contact him at edn-joshua@mindspring.com.

ACKNOWLEDGMENTS

Many thanks to Audio Precision for the use of the SYS-2722 and for the company's ongoing support of the BenchPress projects.

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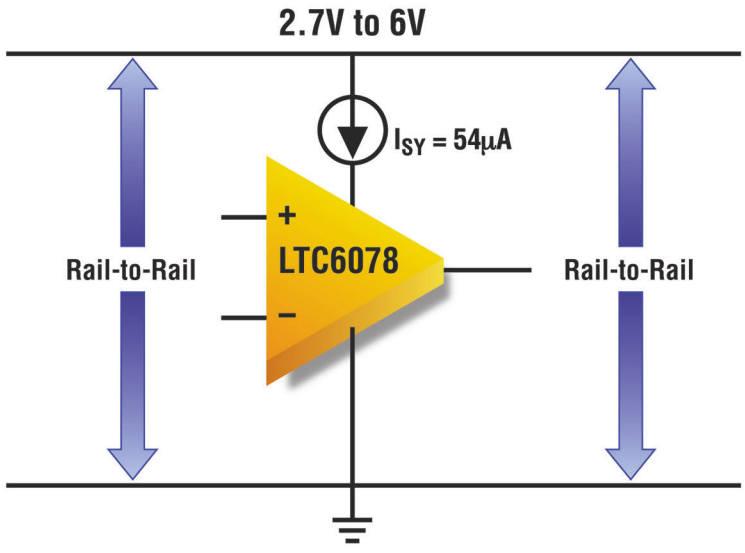
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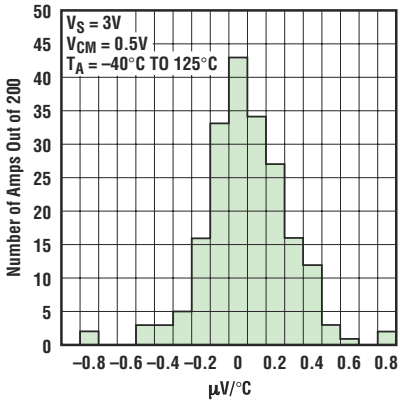
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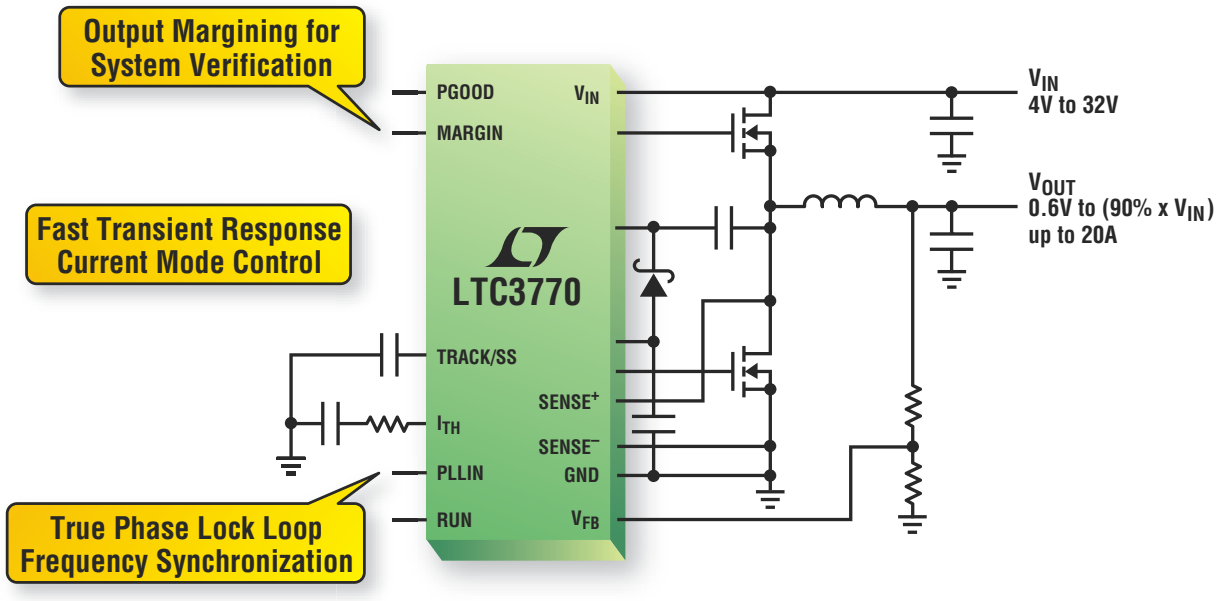
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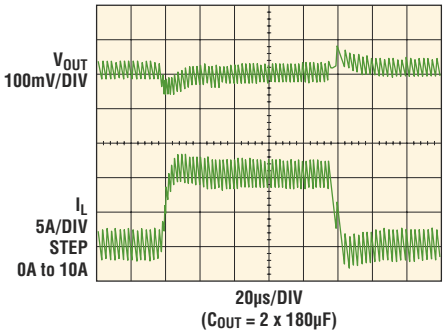
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LINEAR TECHNOLOGY

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designideas

READERS SOLVE DESIGN PROBLEMS

Stereo-amplifier IC's outputs drive multiple loads

Jean-Jacques Avenel, Maxim Integrated Products, Lesigny, France

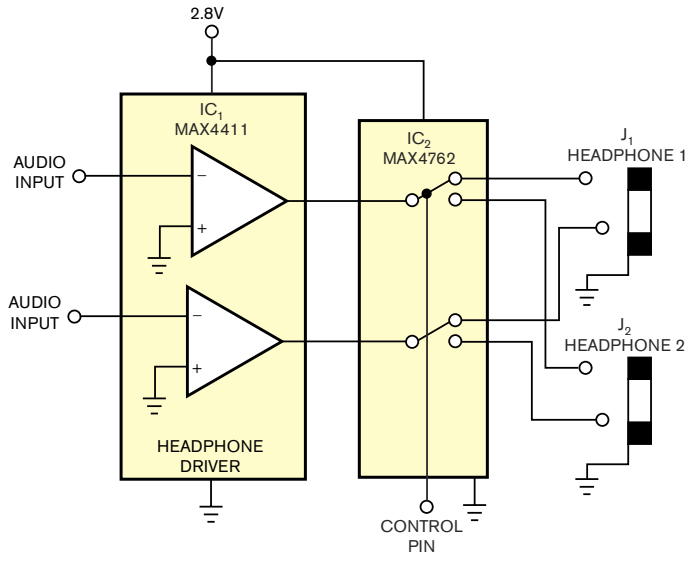


Figure 1 For low values of power-supply voltage, 2.8V maximum, use an analog switch at IC_2 that handles signal amplitudes to $V_{DD}-5.5V$ to direct IC_1's bipolar outputs to the headphone loads.

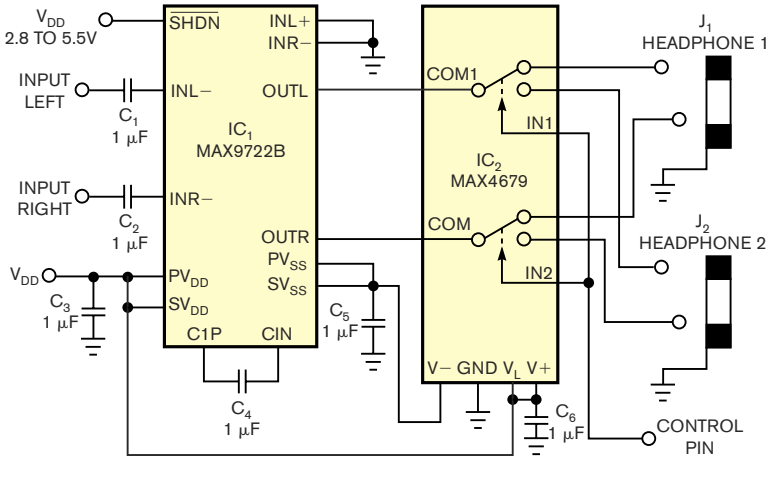


Figure 2 Higher values of V_{DD}, 2.8 to 5.5V, require a different amplifier and a dual-supply-voltage switch at IC_2.

DIs Inside

66 Muscle power drives battery-free electronics

70 FET biasing targets battery-powered PWM applications

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Newer generation, directly coupled stereo-amplifier ICs can directly drive headphones and speakers and thus eliminate bulky and expensive output-coupling capacitors. Many of these amplifiers also include a charge pump for generating an internal negative-supply-voltage rail to produce a bipolar-output swing while operating from one positive-supply voltage. However, if your applications require switching the amplifier's output between two or more headphones or other loads, you cannot necessarily use a simple electronic analog switch. Many analog switches can't handle a signal that makes excursions above the positive-power-supply voltage, V_{DD}, or below ground. Depending on V_{DD}'s maximum value, you can apply one of two approaches.

If V_{DD} falls below 2.8V (**Figure 1**), choose a switch for IC_2 such as Maxim's MAX4762, which handles negative signals down to V_{SS} of −5.5V, where V_{DD} can range from 1.8 to 5.5V with a typical on-resistance of 0.6Ω. If V_{DD} falls between 2.8 and 5V, use a dual-supply, low-on-resistance switch, such as Maxim's MAX4679 at IC_2 (**Figure 2**), along with a different stereo amplifier, such as the MAX9722B, IC_1, to handle the higher V_{DD}. For the switch's negative supply, you can use the nega-

tive voltage generated within the MAX9722B to eliminate the need for an additional charge-pump-power-supply circuit.

To enhance a mobile-telephone design, you can use a stereo-headphone jack to accommodate a hands-free combination earphone and microphone. You use the stereo jack's tip connection as the headphone contact, the ring contact for the microphone, and the shell contact as the common connection to ground (**Figure 3**). When you connect the hands-free combination, you must also turn off one channel of headphone amplifier IC_1. Although the MAX4411 amplifier offers an individual-channel-shutdown feature, the device's outputs present an impedance of 2 kΩ to ground when you switch it off.

An electret microphone capsule typically includes an open-drain JFET-output circuit that typically requires a 2-kΩ resistor, R_1, which connects to a low-noise, positive-supply voltage of approximately 2V. The resistor provides dc bias to the JFET and allows the microphone capsule's audio-output signal to appear on the output terminal. In most applications, the microphone's output connects directly to a high-impedance, low-noise amplifier, IC_3, by ac coupling of capacitor C_1.

The amplifier's 2-kΩ-to-ground off-impedance would heavily load the microphone and halve its dc bias, moving it out of its optimum operating range and reducing its output and SNR. Adding analog switch IC_2 between the microphone and the headphone amplifier's output maintains the microphone's bias and resistive load. EDN

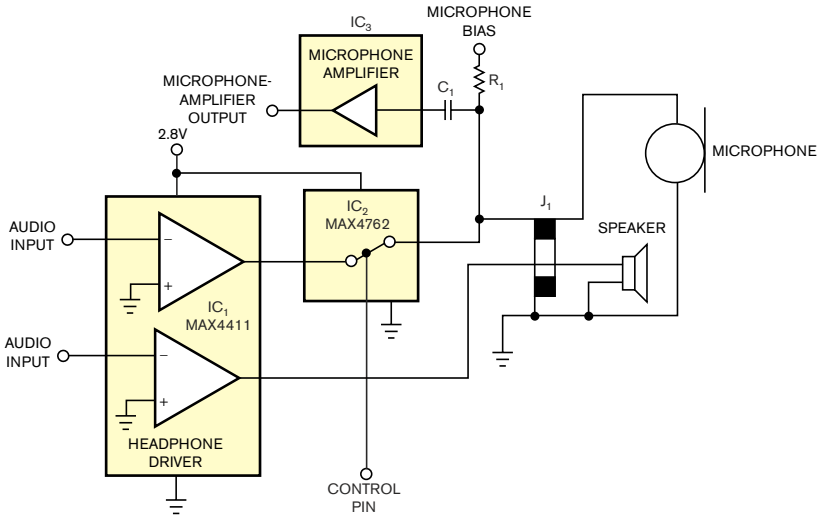


Figure 3 When using a hands-free microphone/earphone kit as an alternative to stereo headphones, add the circuitry shown to avoid loading the microphone's output with the headphone-driver amplifier's output.

Muscle power drives battery-free electronics

Alexander Bell, Infosoft International Inc, Rego Park, NY

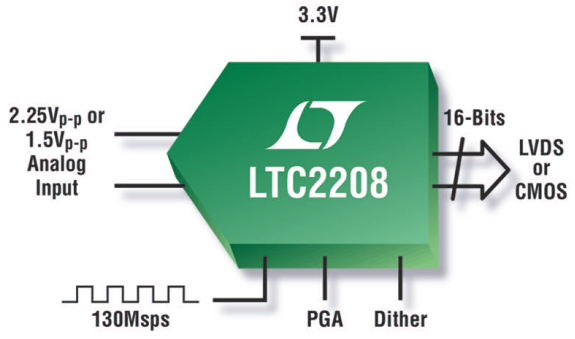
Recent developments in electric-double-layer-capacitor technology have made it possible to replace rechargeable batteries in certain secondary-power-storage applications (**Reference 1**). Capacitors offer significant advantages over rechargeable batteries, including a practically unlimited number of charge/discharge cycles, survival of short circuits, and simple charging circuits that require only overvoltage protection. In addition, storage capacitors recharge quickly and pose no toxic-waste-disposal problems when the product reaches the end of its service life.

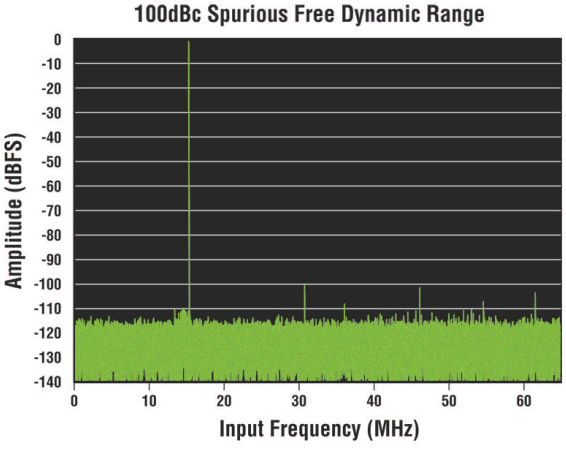
This Design Idea extends an earlier one by describing a muscle-power-driven capacitor charger. The combination of a muscle-powered electrical generator and a high-value capacitor provides a highly autonomous and environmentally clean power approach for emergency equipment and survival kits. Applications of such an alternative "renewable" energy source span a range of modern portable electrical and electronic devices, including cellular phones, MP3 players, AM/FM radios, PDAs, handheld PCs, and flashlights.

A muscle-powered capacitor charger contains only a few components: a storage capacitor, a bridge rectifier, and a voltage-limiting zener diode that protects the capacitor from excessive voltages (**Figure 1**). For practical energy-storage experiments, you can use 1 or 0.47F capacitors with 5.5V maximum ratings, such as those available from NEC-Tokin America (www.nec-tokin.com, **Figure 2**). For more storage, you can use higher capacitance capacitors, such as Elna's (www.elna.co.jp) 100F, 2.5V Dynacaps (**Figure 3**).

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inexpensive, hand-powered flashlight and use its generator as a capacitor charger (**Figure 4**). Also, a variety of manually powered products now appearing on the market offer possibilities for experimentation. For higher outputs, you can use a stationary-bicycle-powered generator. Depending on the individual providing pedaling power, these generators can deliver average powers ranging from 20 to 100W. The hand-cranked flashlight in **Figure 4** originally lit a 2.5V, 0.15A, filament-type bulb, which consumes approximately 0.4W at full brightness. However, measurements show that the generator could deliver more power and could charge a 1F capacitor to 5V in approximately 10 sec. Thus, the following equation calculates the energy, E, stored in the capacitor of value C: $E=\frac{1}{2}C\times V_{MAX2}=12.5J$, and the following equation calculates the average maximum muscle-generated electrical power over time, T: $T_{MAX}=E/T=12.5/10=1.25W$.

You can use the following equation to calculate the effective energy, E_{EFF}, that the capacitor can deliver during its discharge cycle while its terminal voltage changes from maximum to minimum voltage: $E_{EFF}=\frac{1}{2}C(V_{MAX2}-V_{MIN2})$, where V_{MAX2} and V_{MIN2} represent the maximum and minimum operating voltages, respectively, applied to the powered devices. You can connect storage capacitors in parallel or in series. In both cases, make sure that the circuit includes proper overvoltage protection for the capacitors. To obtain additional voltages, you can add a dc/dc switched regulator to produce stable output voltages.

Important design considerations relate to the maximum voltage and current ratings of the diode-bridge rectifier and the zener diode, D_Z. Experimental measurements on the hand-cranked generator yield the following approximate values for its open-circuit voltage: maximum voltage of 10V rms, peak voltage of 14V, and maximum short-circuit current of 200 mA rms. For this application, an inexpensive bridge rectifier with 20V minimum peak-inverse voltage and 0.5A minimum forward current provide adequate margins. D_Z's breakdown-voltage rating should be slightly lower than the storage capacitor's maximum working voltage, and the diode's power rating—2W in this application—should exceed the product of the generator's maximum output current and the zener's conduction voltage. EDN

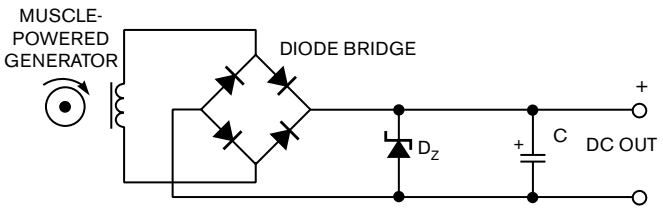


Figure 1 This charger circuit for storage capacitor C requires few additional components: a diode-bridge rectifier and an overvoltage-limiting zener diode.

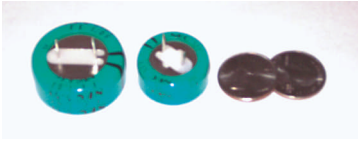


Figure 2 Supercapacitors from NEC America provide 1F (left) and 0.5F of storage at 5.5V maximum and occupy little pc-board area.



Figure 3 These 100F, 2.5V Dynacaps from Elna approximate standard electrolytic capacitors in volume.

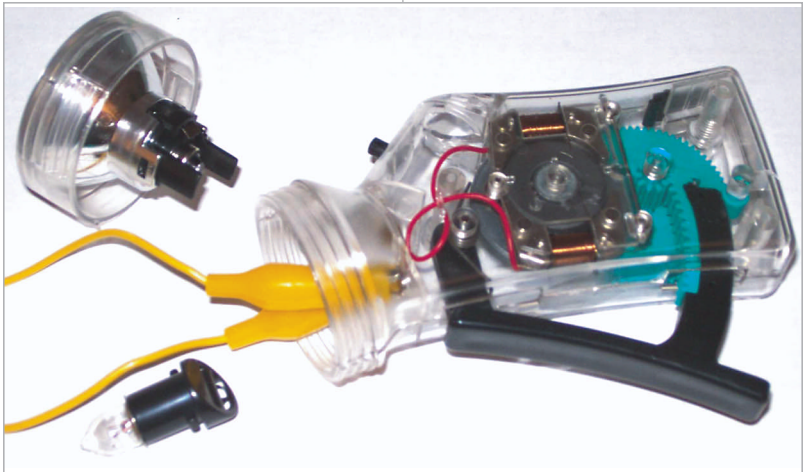


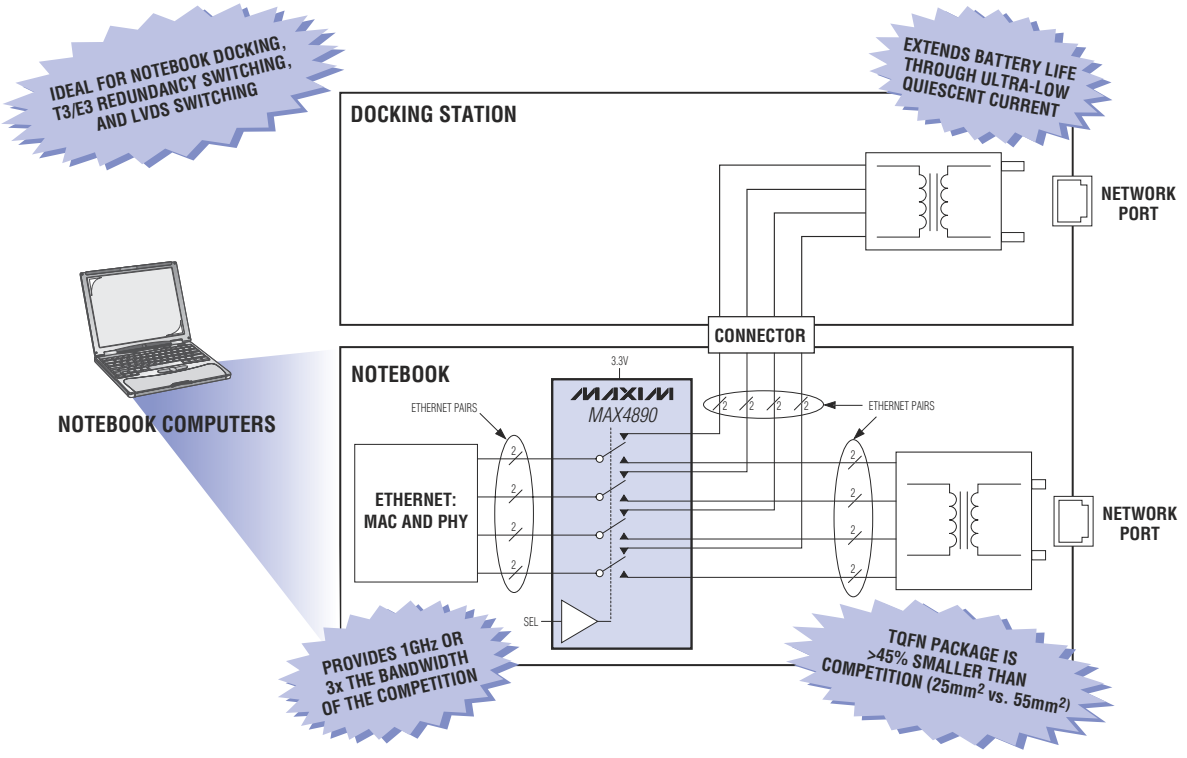
Figure 4 A hand-cranked flashlight's electrical generator serves as a muscle-powered charger for a high-capacity storage capacitor (lower left).

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1 Bell, Alexander, "Single capacitor powers audio mixer," *EDN*, March 14, 1997, pg 80, www.edn.com/archives/1997/031497/06DI_04.htm.

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FET biasing targets battery-powered PWM applications

Steve Franks, Franks Development LLC, Tucson, AZ

Many PWM (pulse-width-modulated) applications, such as Class D audio amplifiers, require symmetric drive circuitry. Comprising complementary N- and P-channel FET devices with gates and sources connected, the textbook CMOS pair in **Figure 1** provides a low-impedance path to either the positive or the negative power supply and can directly drive a logic-level N-channel FET. Direct coupling of the CMOS pair to the logic driver works well in PWM systems in which the controlled devices operate at the same voltage as the logic circuits. However, raising the output FETs' power-supply voltage while driving the gates from lower voltage logic results in the P-channel device's remaining in conduction because of the difference between supply voltages.

To achieve an off-state, an amplifier's P-channel FET's gate must go to the positive-supply rail. Complementary-CMOS logic-level drivers can't accommodate the amplifier's high positive-supply voltage, and alternatives, such as using commercial FET drivers and operational-amplifier level-shift circuits, add cost and complexity. You can add an external high-voltage N-channel FET to drive the P-channel-amplifier FET's gate (**Figure 2**). However, capacitive loading imposes an exponential-rise characteristic on the drive waveform, leaving the P-channel FET in its linear operating region for an extended period and thus limiting switching frequency and causing significant power losses in the cascaded FETs.

Current-generation PWM systems can operate at relatively high switching frequencies and, as **Figure 3** shows, allow you to use a dc-blocking coupling capacitor, C_B, between the logic-level driver's output and the P-channel output FET's gate. Resistive divider R_1 and

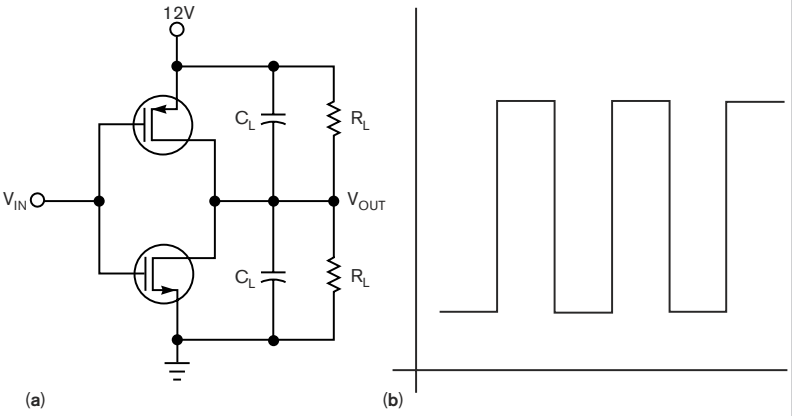


Figure 1 The textbook complementary-CMOS pair (a) produces a clean output waveform with fast on/off transitions (b).

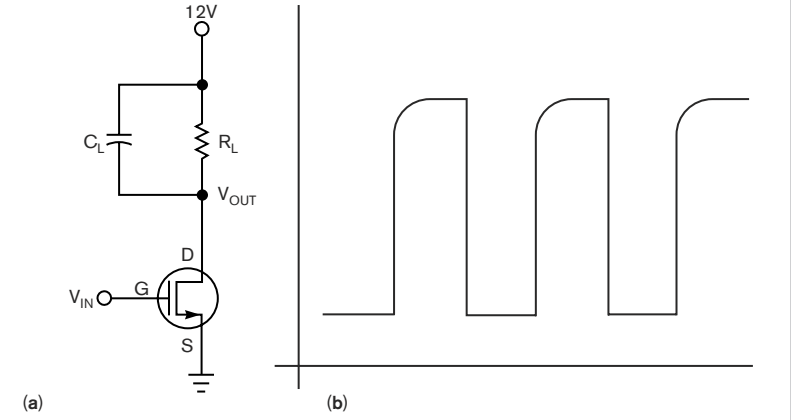


Figure 2 An N-channel FET driver (a) has output that exhibits an exponential rising edge on shutoff.

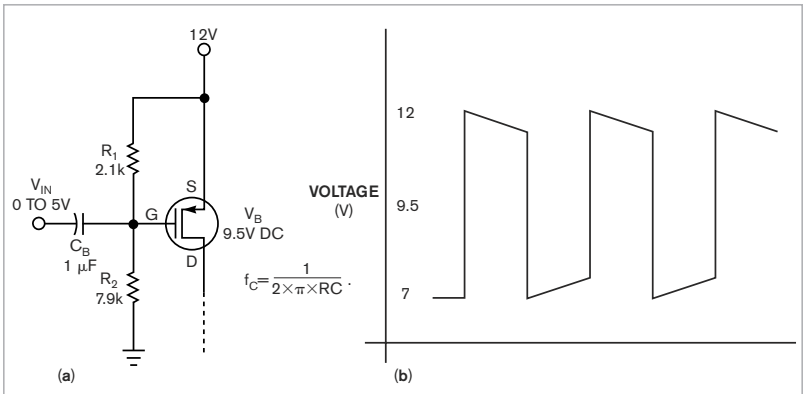
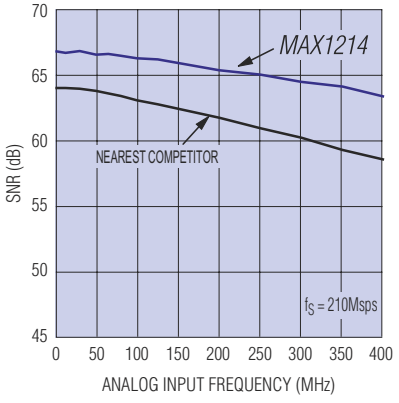


Figure 3 Adding resistive bias and capacitive coupling to an N-channel MOSFET (a) improves transition times but introduces waveform droop during on or off intervals (b).

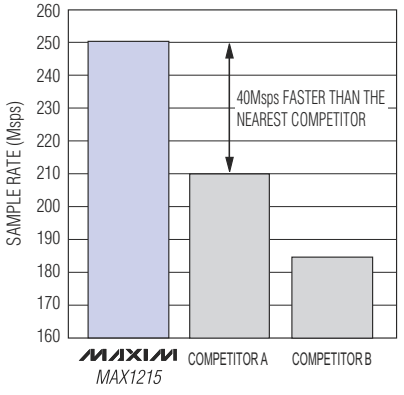
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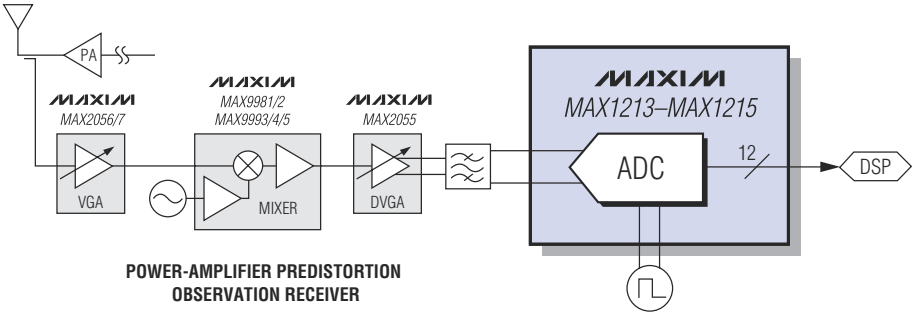
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R_2 applies a dc bias to the output FET's gate that's equal to the difference between the output power-supply voltage and the midrail logic voltage. For example, in a 12V Class D PWM audio amplifier driven from a 5V microcontroller, bias the P-channel FET's gate at 9.5V (12V−5V/2). Use the specified FETs for logic-level gate drive as output devices because other FETs don't exhibit nominal I_{DS} characteristics at gate drives of 5V or lower.

Battery-powered amplifiers with resistive-divider output-stage bias introduce an additional complication. As battery voltage decreases, so does bias. Instead, you can use a voltage-reference IC or a zener diode, D_1, to provide a constant bias voltage regardless of supply-voltage variations (**Figure 4**). This technique consumes less power than a purely resistive divider and offers more flexibility in coupling-capacitor selection to reduce waveform droop. Based on Texas Instruments' TPA2010 PWM power-amplifier IC (**Reference 1**), a Class D audio power amplifier boosts the TPA2010's 2.5W differential output to more than 200W rms into an 8Ω load (**Figure 5**).EDN

REFERENCE

1 TPA2101D1 data sheet, http://focus.ti.com/lit/ds/symlink/tpa2010d1.pdf.

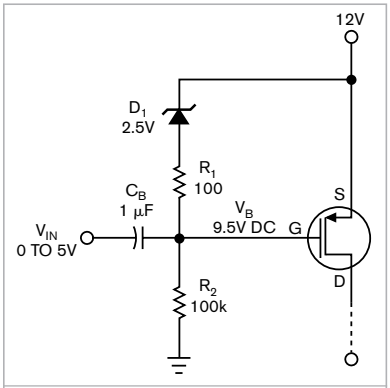


Figure 4 Inserting a zener diode into the bias divider allows optimization of the coupling capacitor's value and the P-channel device's bias voltage for logic-level drive.

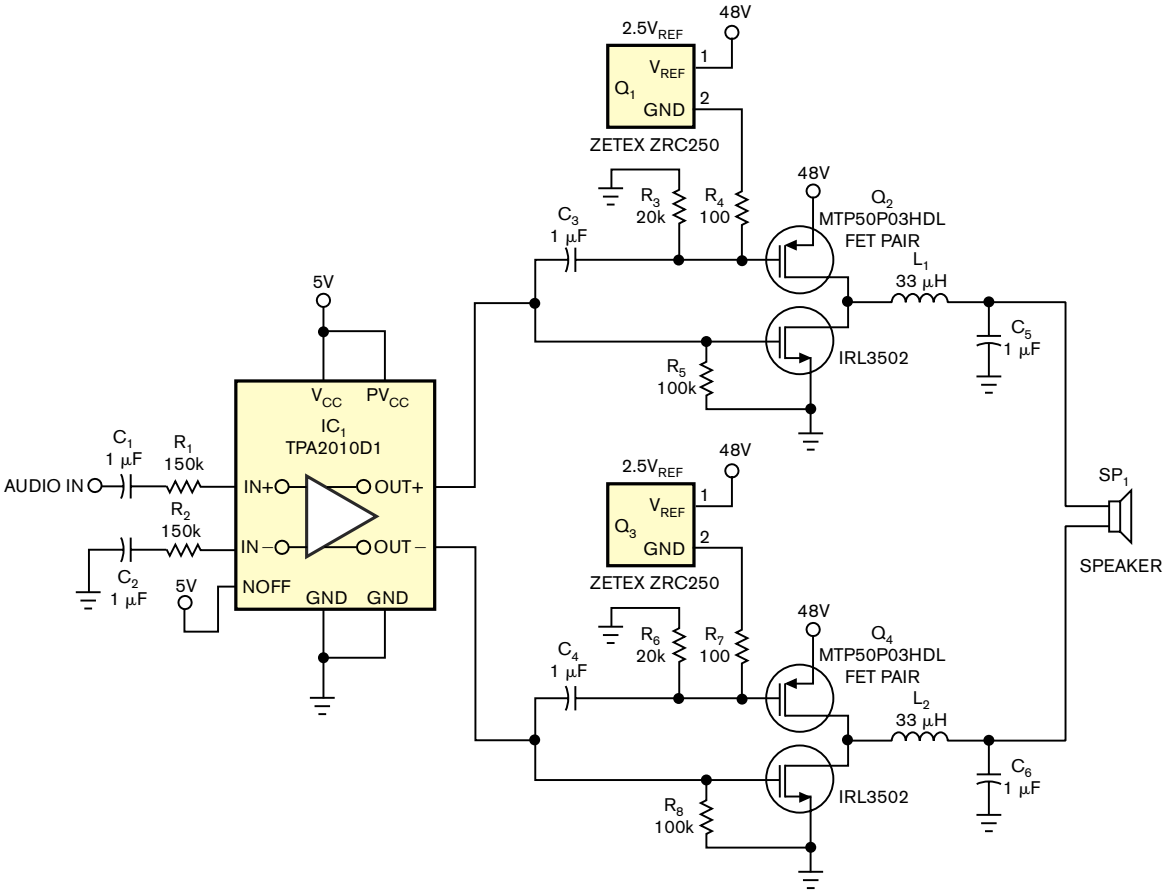


Figure 5 This Class D audio amplifier boosts its driver's output to 200W rms for a 48V power supply.

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DESIGN NOTES

Monolithic Converter Drives High Power LEDs – Design Note 376

Keith Szolusha

Introduction

High power LEDs are quickly expanding their reach as the lightsource of choice for flat panel computer and TV monitors, TV projection, signage, portable lights and automotive interior, trim and brake lighting. The input voltage and LED voltage combinations across these applications are as diverse as the applications themselves, precluding the ability for a single topology to satisfy the needs of them all. Nevertheless, all LED drivers, whether buck, boost, buck-boost or SEPIC must regulate a constant LED current, regardless of input and output voltages. Now a single switching regulator with the ability to be configured in a large variety of topologies for high power constant LED current is available.

The LT®3477 can drive high power LEDs at constant current in any of the topologies stated above. It is a current mode, 3A DC/DC step-up converter that incorporates dual rail-to-rail current sense amplifiers and an internal 3A, 42V switch. It combines a traditional voltage feedback loop and two unique current feedback loops to operate as a constant-current and/or constant-voltage source. The floating rail-to-rail current sense amplifiers allow for both ground-referenced and floating LED solutions in different topologies, along with the added benefit of inrush current or short-circuit protection.

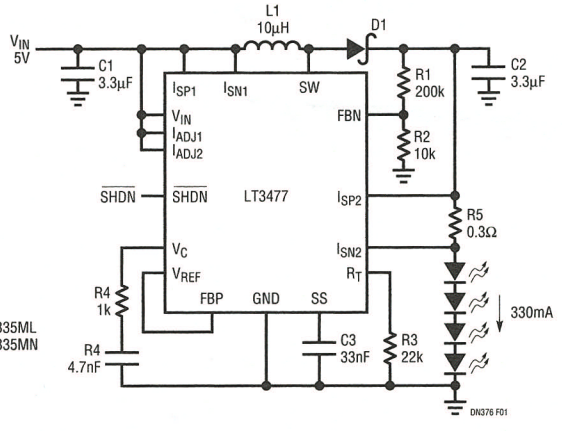
Both current sense voltages are 100mV and can be adjusted independently using the I_{ADJ1} and I_{ADJ2} pins. Efficiencies of up to 91% can be achieved in typical applications. The LT3477 features a programmable soft-start function to limit inductor current during start-up. Both inputs of the error amplifier are available externally, allowing positive and negative output voltages. The switching frequency is programmable from 200kHz to 3.5MHz through an external resistor. It comes in two thermally enhanced packages: a 20-pin (4mm × 4mm) QFN and a 20-pin TSSOP.

Boost Driver

The LT3477's internal ground-referenced 3A NPN power switch is most commonly used for boost applications. Figure 1 shows a 5V to four 1W LED boost converter with open LED protection and 330mA constant LED current. The constant current is regulated using a current sense amplifier and a 0.3Ω sense resistor. The feedback voltage amplifier is only used for overvoltage protection in case the LEDs are removed from the circuit.

The forward voltage of the four LEDs ranges from 12V to 16V. The input voltage range is 2.5V (minimum LT3477 input voltage) up to just below the LEDs' forward voltage. The LT3477 can drive more LEDs as long as the peak switch current remains below 3A.

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C1: TAIYO-YUDEN LMK316BJ335ML
C2: TAIYO-YUDEN TMK325BJ335MN
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L1: TOKO A915AY-100M

Figure 1. 330mA Boost LED Driver with Open LED Protection

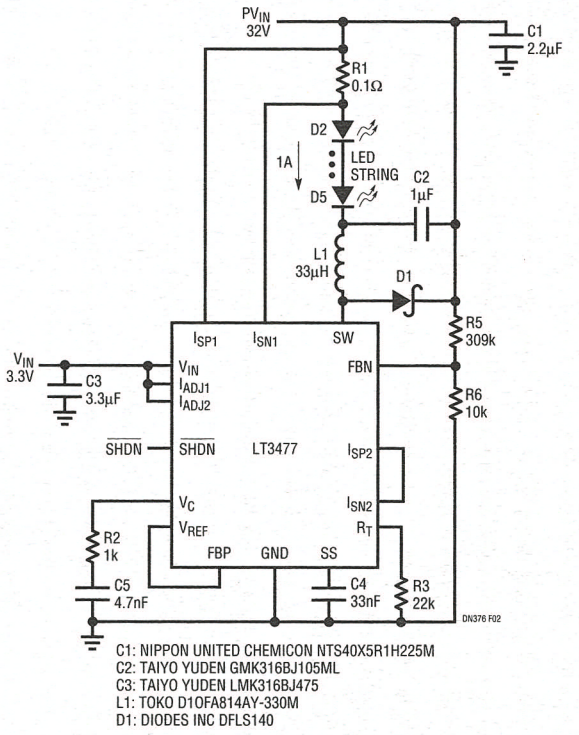


Figure 2. 1A Buck LED Driver

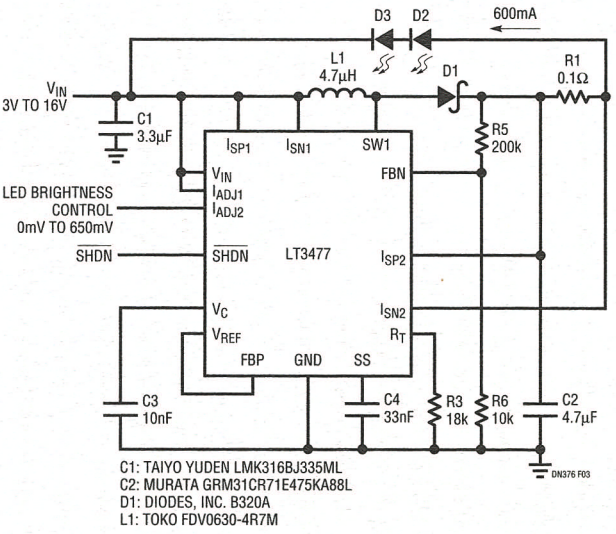


Figure 3. Buck-Boost LED Driver

Buck Driver

LEDs are best driven with a constant current source, but unlike most system loads, they do not have to be ground referenced. Therefore, the LT3477 with its floating current sense amplifiers can be converted into a buck LED driver with low LED ripple current. Figure 2 shows a 32V input voltage buck converter driving a string of 1A LEDs. The LEDs are tied to the input source through a sense resistor and the typical output Schottky catch diode is tied back to V_{IN}, converting the boost IC to a monolithic buck LED driver. Once again, the feedback voltage amplifier is only used for overvoltage protection—this time on the input—to prevent damage to the 42V switch. In buck mode, the V_{IN} pin need only be tied to a 3.3V or 5V source for maximum efficiency, and to keep it below its absolute maximum rating of 25V. The dimming I_{ADJ} pin functions work the same in buck mode as boost mode, reducing the LED current proportionally.

Buck-Boost Driver

If the battery range lies both above and below the forward voltage range of the LEDs, the LT3477 can simply be converted into a buck-boost converter as floating current sense amplifiers allow the LED string and its series sense resistor to be tied anywhere in the circuit. By altering the typical boost LED driver application so that the LED string returns to V_{IN} as opposed to ground, step-up/step-down capability is provided.

Conclusion

The LT3477 is a versatile, monolithic boost, buck, and buck-boost or SEPIC LED driver with a high power 3A, 42V switch. It can also be used for boost or SEPIC voltage converters requiring inrush or short-circuit protection. Two floating current sense amplifiers and a ground-referenced voltage feedback amplifier help give the LT3477 its high level of versatility. The externally programmable switching frequency, a shutdown pin, LED current dimming adjustment and a single soft-start capacitor satisfy the additional requirements of LED drivers and boost/SEPIC regulators.

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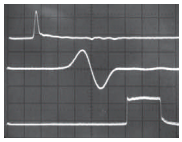


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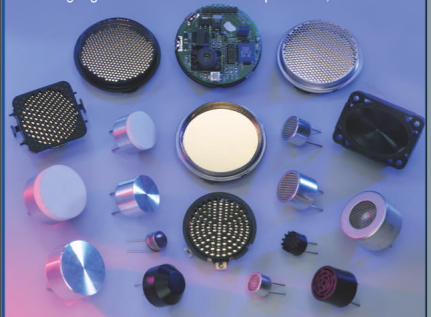
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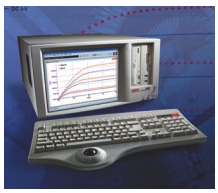
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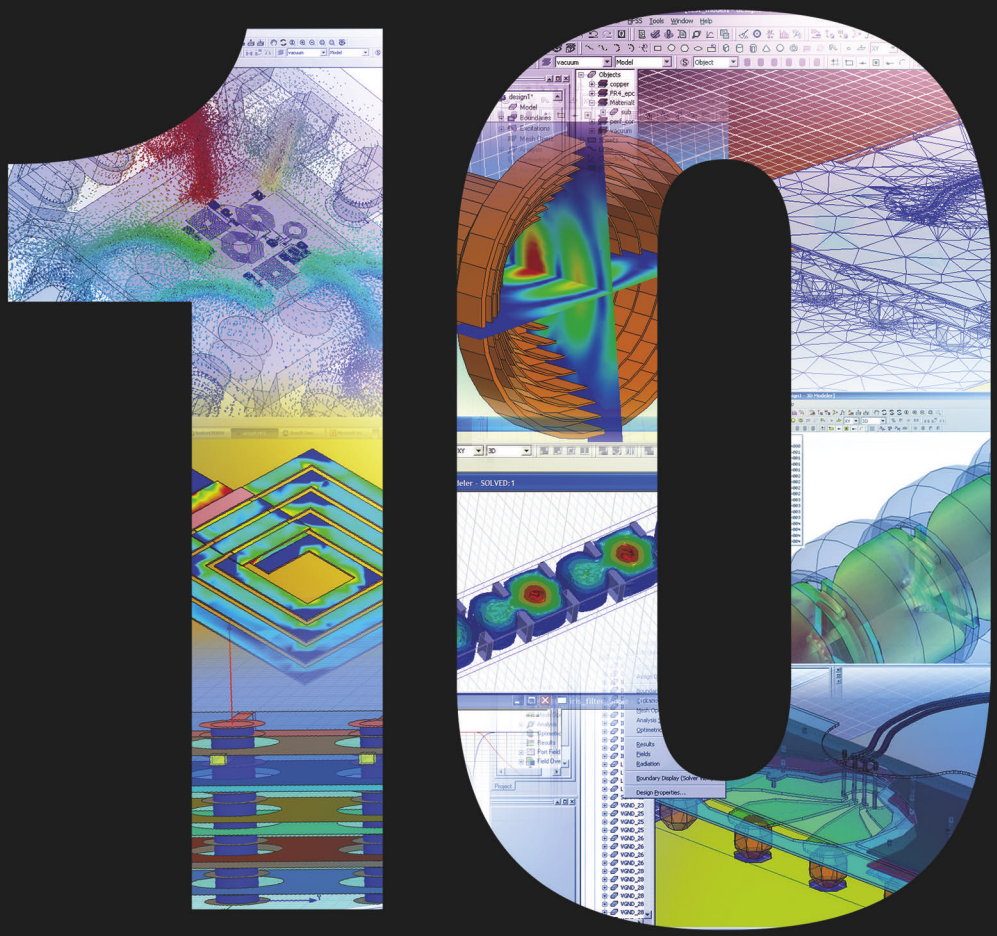
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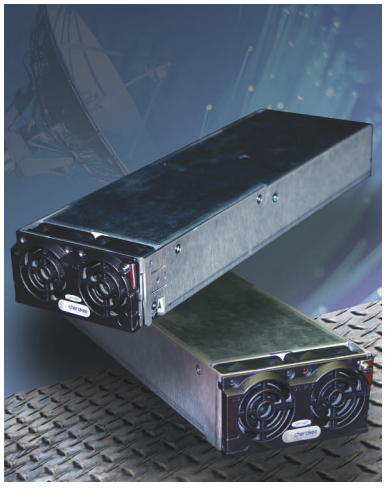
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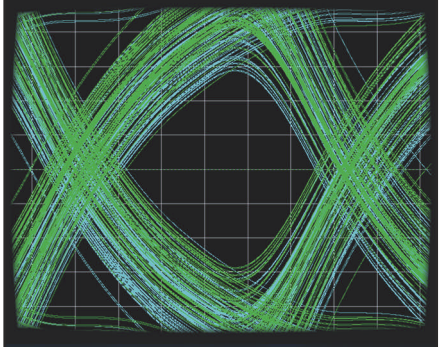
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TimeSys Corp, www.timesys.com

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The G2 line of rugged, high-resolution PMC graphics controllers uses advanced display- and video-capture capabilities for demanding applications. The devices feature ATI Technologies' Mobility Radeon 9000 (M9) graphics processor with 2- and 3-D acceleration; OpenGL and DO-178 support; and Linux, Integrity, VxWorks, and Windows XP support. Commercial-temperature, extended-temperature, and conduction-cooled versions are available. The device also offers optional resources, including built-in video-capture types and formats and dual-display support. The G2 costs $2200.

SBS Technologies, www.sbs.com

Eight-slot CompactPCI subsystem uses redundant power supplies

With a 64-bit, eight-slot, 6U backplane and redundant power supply, the high-performance cPCIS-6418U 4U rack-mount CompactPCI enclosure dedicates one slot to the system CPU board and seven slots to peripheral boards. It supports a PICMG 2.5-compliant H.110 CT Bus. A front-access, hot-swap cooling system handles CPU heat ventilation and high-density computing. The subsystem uses hot-swappable 500W+200W redundant power supplies with a universal ac input. With a 4U enclosure, the cPCIS-6418U costs $2695.

Adlink Technology Inc, www.adlinktech.com

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productroundup

EMBEDDED SYSTEMS

Serial-RapidIO boards suit embedded-system applications

Comprising a 19-in., 7U rack and eight VME64x slots with P0, the PowerMP4-60's board configurations of eight PowerPC G4 7457 CPU boards operate at 1 GHz, supplying 60 Gflops of computing power. The system also includes a PentXM board operating at 1.6 GHz. A 2.4-Gbyte/sec bandwidth in the serial-RapidIO switch fabric allows for interconnection in all directions, sustaining maximum throughput between processors. The devices connect through a low-latency, high-bandwidth RapidIO network, and designers can route the PowerPC nodes through the backplane using the P0 or front-panel connectors. The system also features a front-panel-data-port stage that acquires data at 100 Mbytes/sec, MPI (Message Passing Interface) communications, and SNMP control and monitoring. Third-party development tools include the Spyker system-trace analyzer, the Totalview debugger, and the VSIpro math library. Moreover, the PowerMP software package includes an integrated development environment with tools such as compilers, configuration managers, debuggers, and trace tools. The boards operate under Linux 2.4, and the PowerPC cluster will operate under Linux SMP 2.4, LynxOS 4.0, or VxWorks 6.1. The PowerMP costs $18,000.

Thales, www.thalescomputers.com

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YESTERDAY'S HYPE MEETS TODAY'S REALITY

IBM 5150



IBM DISPLAYWRITER



IBM 5120



IBM 5110



STATS IBM's first PCs: $1565 to $2665 / 200,000 sold in first year / 28 lbs with two disk drives

IBM 5150 PC started the modern electronics revolution

Even though consumer electronics and mobile handsets have long since eclipsed it, the PC can rightfully take credit for creating the modern electronics industry as we know it. IBM introduced the 5150 PC on Aug 12, 1981, but its predecessors—the 5110, the 5120, and the Displaywriter—offered glimpses of it. It first became popular in corporate offices and then spread to all businesses and into the home. The fact that the Apple II had preceded the PC by four years didn't matter. IBM so dominated business computing, it was assumed that the 5150 would snuff out plucky upstarts such as Apple. After many twists and turns, Apple today still makes new PCs, whereas IBM's inability to profit from them after more than 20 years of trying led to this year's sale of IBM's PC business to Lenovo.

Sales of PCs worldwide this year should pass 200 million for the first time, according to IDC. Less than one-third of those will sell in the United States; of those, nearly 40 million will go to commercial enterprises, and the rest will go to consumers. After years of double-digit growth, annual sales will fall 9.1% worldwide in 2006, forecasts IDC. To read about the 5150's history and IBM's original press announcement, go to www-03.ibm.com/ibm/history/exhibits/pc/pc_1.html or www-03.ibm.com/ibm/history/documents/pdf/pcpress.pdf.—by John Dodge

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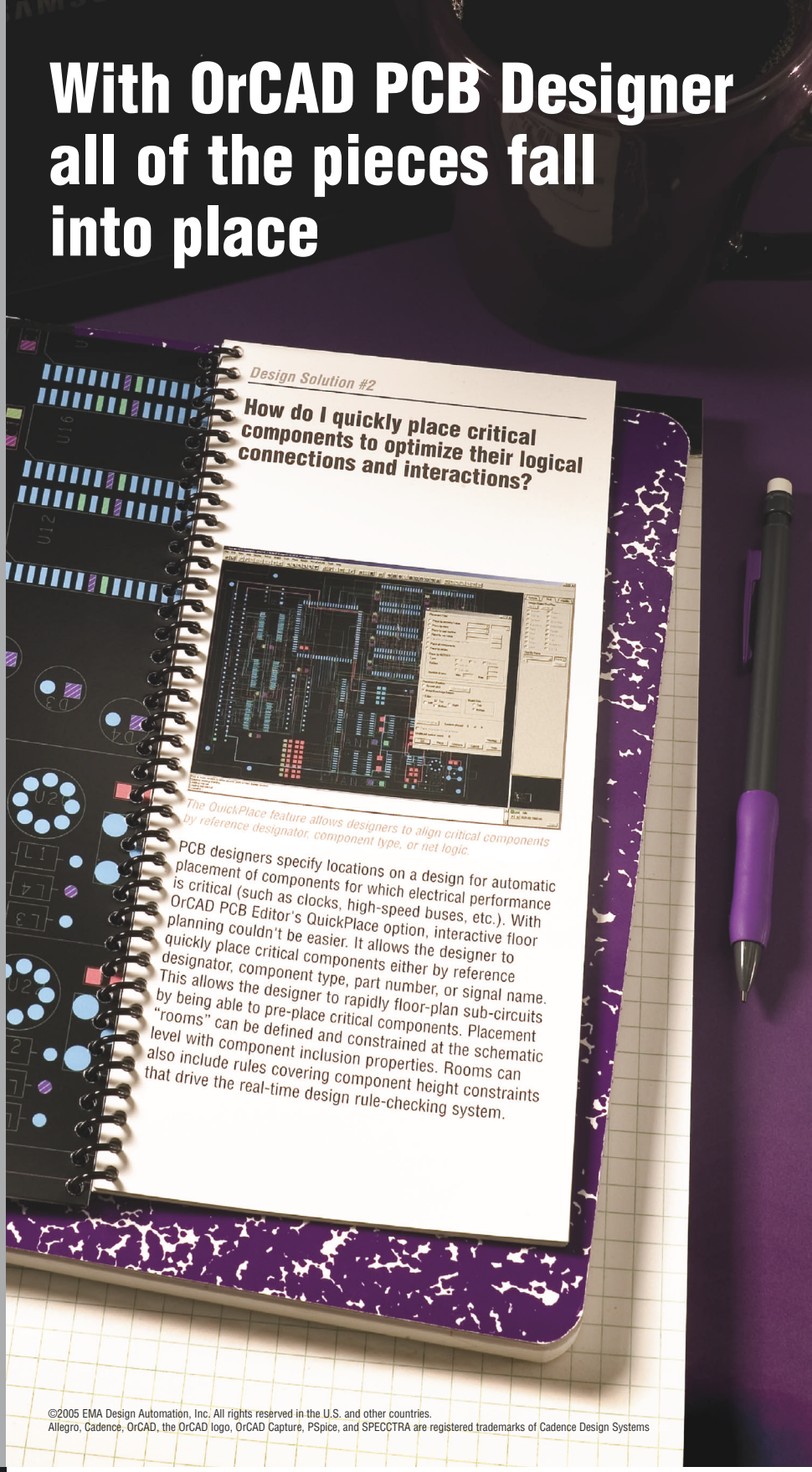
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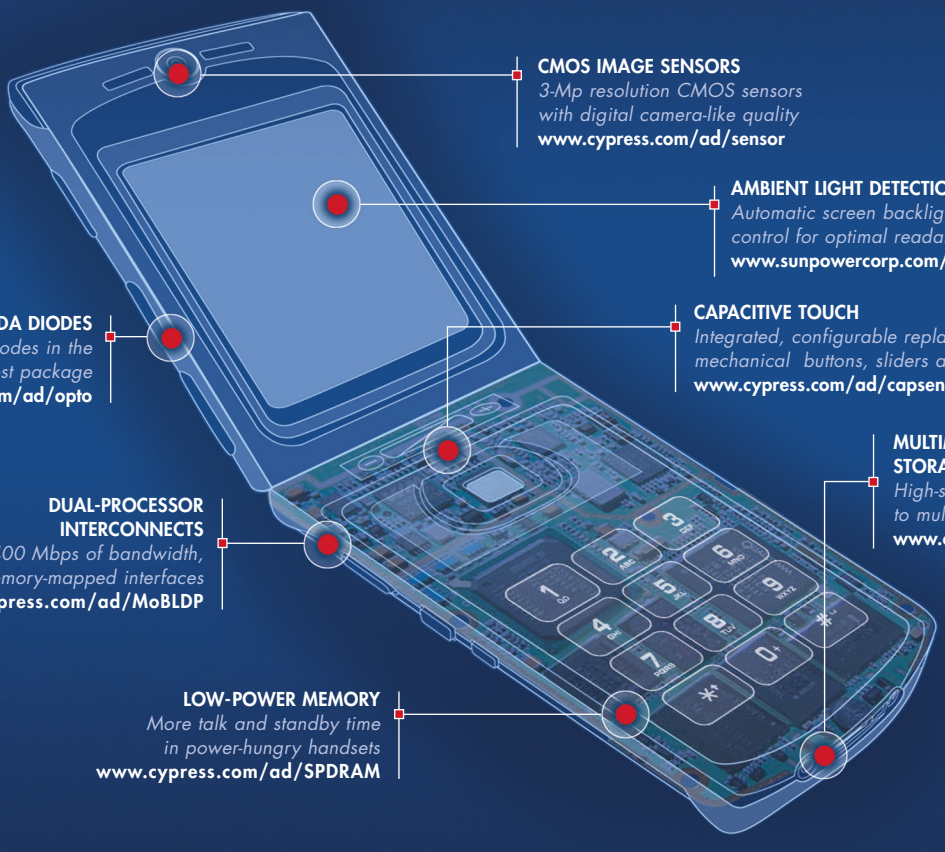


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